COMPUTATIONAL BIT ERROR RATE ANALYSIS OF AN ALL OPTICAL PACKET SWITCH BASED ON FIBER LOOP BUFFER MEMORY

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by

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CERTIFICATE

This is to certify that the thesis work entitled "Computational BIT ERROR RATE ANALYSIS OF AN ALL OPTICAL PACKET SWITCH BASED ON FIBER LOOP BUFFER MEMORY" by Dhaval Kumar Deshmukh, Roll No. 9810417 has been carried out under my supervision and the same has not been submitted else where for any degree or diploma.

March 21, 2000

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Abstract

The growth of existing and new services will creat large increase in traffic flow in Telecommunication Networks. This requires high capacity networks and nodes. Nodes of such networks will be fed by input links with bit rates ranging from 155 Mbps to 2.5 Gbps which requires switching capacities of several Tbps. In the existing networks routing and multiplexing is performed electrically, optics being confined to transmission only. Although electronic technology can achieve high switching speeds, but it is not well matched to transmission bandwidth of fiber optic links, and the switch bandwidth could become a bottleneck. One possible solution is all-optical packet switches.

Implementing static buffers is a problem for all optical switches and various methods have been proposed to store packets in optical mode. In this work, Fiber Loop Buffer Memory switch architecture has been considered in which multiple packets can be stored on different wavelengths in a fiber loop. Inside the loop, SOA switches are used along with a Multiplexer and Demultiplexer both of which significantly attenuate the signal. An EDFA is used to amplify the signal in loop. EDFA and SOA introduce ASE noise. These noises deteriorate the Bit Error Rate at the receiver. In this work Bit Error Rate analysis of this switch has been carried out, using the computational models of different components used in the switch and by having a receiver at the output of the switch. 8×8 and 16×16 switches are considered for different number of wavelengths, under different load conditions. It leads to the conclusion that higher the number of packets in loop, better is the BER performance at the receiver, and hence higher number of recirculations possible in the loop. Further the gain in loop should always be maintained equal to loss for optimal switch performance i.e. to maximize the recirculation limit.

ACKNOWLEDGEMENT

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Words are not enough to explain my feelings towards my parents. I always found them standing by my side during my hard days.

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LIST OF ABBREVIATIONS

FLBM - Fiber Loop Buffer Memory

ATM - Asynchronous Transfer Mode

SDH - Synchronous Digital Hierarchy

SOA - Semiconductor Optical Amplifier

EDFA - Erbium Doped Fiber Amplifier

TWC - Tunable Wavelength Converter

TF - Tunable Filters

MUX - Multiplexer

DEMUX- Demultiplexer

ASE - Amplified Spontaneous Noise

ESA - Excites State Absorption

WDM - Wavelength Division Multiplexing

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Chapter 1

INTRODUCTION

With the emergence of broadband services like video conferencing, multimedia applications, video on demand etc, the demand for networks with very high capacity is increasing. It is expected that in next 15 years the traffic demand on core telecommunication networks will grow ten to hundredfold [1]. These predictions have resulted in extensive research in high capacity transmission systems and networks. Current network technologies such as transmission using the synchronous digital hierarchy (SDH) and switching using asynchronous transfer mode (ATM), are expected to meet the short term growth in demand but in longer term electronic systems are expected to become increasingly complex and costly. In future most of the networks will be fiber optic networks, consequently network designers will look towards optical switches. Optical switches provide much less clock skew between input and output path. Further, radiation from electronic components (which implies electromagnetic interference) will be much less as high bit rate payload will remain optical through out the network

1.1 Switching Technologies

Switching technologies can be broadly classified in to two categories 1 Circuit Switching and 2 Packet Switching.

1.1.1 Circuit Switching

In the classical approach of circuit switching a physical path is established for the complete duration of the connection. This has been used in Telephone Networks for a long time and is still used in Narrowband Integrated Service Digital Network (NISDN) The physical path may be a copper cable, radio, infrared, a microwave link or fiber cable where thousands of channels are multiplexed Once a path has been set up, a dedicated path between both ends exist untill the call is finished An important property of circuit switching is the need to setup an end to end path before any voice, video or data transfer can take place This requires some amount of time which is called the call setup time.

1.1.2 Packet Switching

With packet switching no physical path is setup in advance, instead when a sender has some data to send, it sends in the form of a packet along with a header attached to it to the nearest switching node. The header contains source and destination addresses and some control information. The packet is then routed by the node according to the information in the header. These packets are buffered in the memory of switching node if there is any contention for the output line, through which the packet is to pass.

The packet size has an upper limit The upper limit on the packet size ensures that no user can monopolize on any transmission line for very long. This makes the network

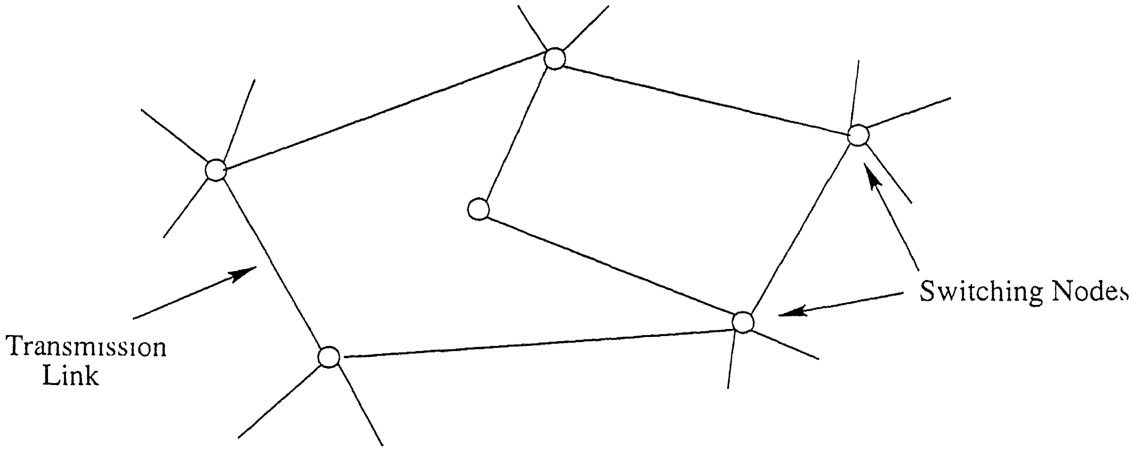

Figure 1.1: Packet Switched Network

suitable for interactive traffic. Packet switching also offers the advantages of reduced delay and improved throughput over circuit switched networks.

1.2 Model of a Packet Switched Network

Model of a packet switched network is as shown in Fig 1 1 A packet switched network can be seen as a hierarchy of switching nodes. Each of these switching nodes is connected to several other switching nodes by high bandwidth links At the lower level, a number of hosts are connected to these switching nodes by relatively lower bandwidth links. Packets sent by the hosts are routed by the switching nodes to other switching nodes according to their header.

The network may be connection-oriented or connection-less type. For connection-oriented networks a virtual path is setup between source and destination hosts prior to data transfer. The switching nodes maintain a routing table which contains entries for all active channels through the node. This fixes path for all packets between any two hosts For connection-less networks no path is setup in advance The switching nodes keep some permanent entries in their routing table and does the routing accordingly.

The packets between any two node may take different paths to reach to the destination host

1.3 Switching Node

The performance of a network largely depends on the performance of its switching nodes Switching node architecture can be centralized or distributed [2]. In a centralized switch sources and destinations communicate through switch elements at the switch periphery. Such switches are appropriate for geographically localized communications such as single multiprocessor computing systems or inter-office communications Distributed switches allow sources and destinations to communicate through most or all switch elements and are appropriate for architectures where nodes are geographically separated such as a distributed computing environment or a broadband digital services network. The basic functions performed by the switching nodes are [2,3]

- Routing of packets from switch input to switch output Packet headers are separated from the data at each switch and processed to set the correct switch state
- Flow Control and Contention resolution· Traffic in switch must be regulated to prevent packets from running in to each other and congesting resources. Buffering, Blocking, Dropping and Deflection are examples of the techniques used for contention resolution
- Synchronization: Time alignment of packets at multiple switch input ports in order to correlate the packet positions with actual switching events
- Header regeneration and reinsertion: This should be independent of packet life time in the network.

The general switching node architecture is shown in Fig 1 2

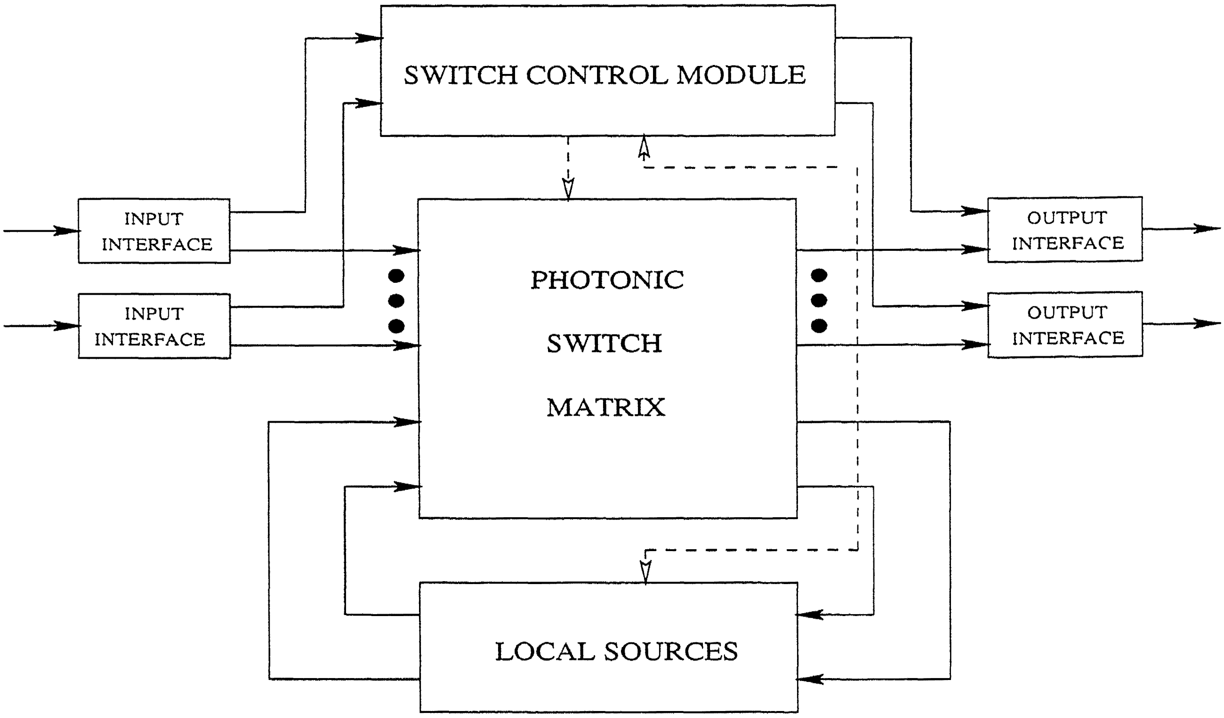

Figure 1.2. Switch node architecture

It consists of mainly three modules [2]. The first one is the Link Interface Module whose functions are signal regeneration, clock recovery and synchronization. The second is Large Switch Matrix through which the packet finds its way to the respective output line of switching node The third one is the Control Processing Module which processes the header and controls the switching operation in the switch matrix. All the decisions regarding packet routings are taken by control module. Local Source block represents hosts which are locally connected to this switching node.

1.4 Elementary Switch Module

Large size matrix fabrication is difficult to realize, therefore they are realized by interconnecting multiple elementary switch modules of limited size in cascade. The size of the elementary switch module is a parameter of switch design

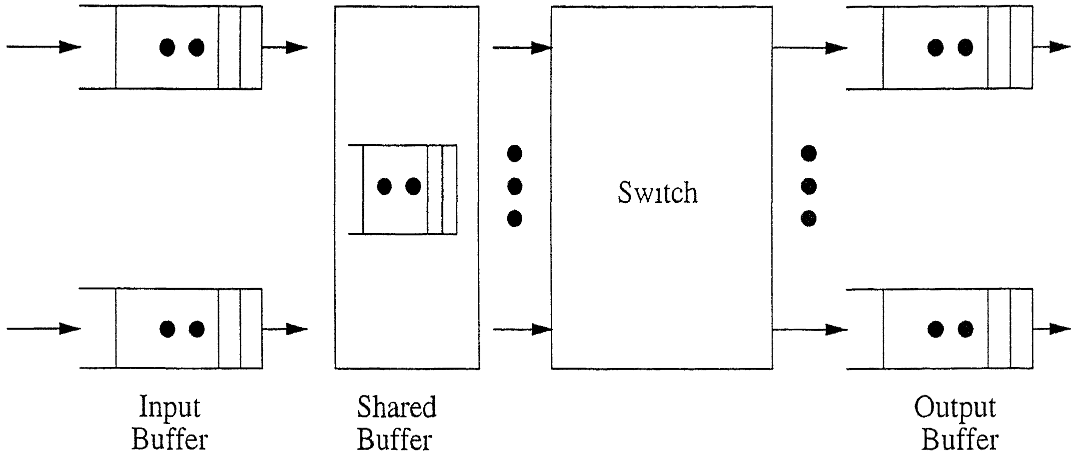

Figure 1.3: Various types of Buffering

1.4.1 Buffering Techniques

In a typical electronic switch, buffers are used for contention resolution and flow control and can be located at different points in the switch A switch with possible buffer locations is shown in Fig. 1 3

Depending on the location of the buffers, the switches are called as input buffered, output buffered or shared buffer switches. The buffer size is choosen to handle the mismatch between the input flow of packets and the estimated output flow

1.4.2 Performance Parameters

There are various parameters which decides the performance of a switch

- Packet Loss Ratio : This is the ratio of the number of packets lost to the total number of Packets arrived in the switch over a long period of time.
- Queueing Delay : This is the amount of time, on an average a packet experiences waiting in the buffer. This decides the total delay for a packet in the network

- Load on the switch : The load on a switch is measured in Erlangs and is defined as the ratio of arrival rate to service rate.

$$Load\ on\ the\ switch = \left(\frac{\lambda}{\mu}\right) \tag{1 1}$$

where $\lambda = Arrival\ Rate$,

and

$\mu = Service\ Rate$. Service time for packet switches is nothing but the transmission time and depends on the packet size. For fixed size packets (like in ATM) service time for a packet is fixed.

- Throughput . The throughput of a switch is defined as the effective arrival rate that can be handled by the switch. This is given as

$$Throughput = \lambda(1 - P_B), \tag{1 2}$$

where $\lambda = Arrival\ Rate$,

and

$P_B = Probability\ of\ Blocking$.

1.5 Optical Packet Switching

Existing packet networks use optical fiber as the transmission link in the backbone but the switching nodes are still electronic in nature. This requires electrical to optical and optical to electrical conversions of the signals at switching node interfaces as the transmission is done in optical mode but switching takes place in electrical mode. This works well for current traffic requirements and data rates but will pose many problems as the data rate increases.

1.5.1 Problems with Electronic Switches

- Fastest data rate supported is based on the basic buffer clock rate Such buffers can not be used for very high data rates due to losses in interconnect and clock skew problem Further, due to higher bit rates, cross talk among electronic components will be high.

- The control processing module must perform all the processing in one packet time therefore the processing speed required is very high. Packet time depends on the packet size so for small packet size, processing speed required is very high

- At high data rate synchronization is also a problem, hence tolerance on clock skew are very tight.

1.5.2 All-Optical Switches

The term All-Optical means that the data portion of the packet is maintained in optical form right from source to the destination, however the header portion of the packet may or may not be optoelectronically regenerated at each switch depending upon the control technique adopted. The switching matrix is designed for optical signals, but the control processing module continues to be operating in electrical mode. This is due to the fact that optical technology is still immature to provide optical signal processors. The packet size has to be kept large so that the control processing module gets sufficient time to process the header and hence the control processing module need not work at a speed equivalent to data rate but at a speed much less than that.

Following are the issues with optical packet switches .

- Optical data can not be stored statically like the electrical data that can be stored in the main memory for as long as required, and must be processed and switched

on the fly. Switch architectures with different buffering techniques have been proposed in literature. They are discussed in the next section

- For electronic switches routing and control techniques were developed that heavily utilized memory for synchronization, flow control and contention resolution since the electronic memory cost is very low and the link bandwidth was relatively large But the situation is opposite for optical switches as the optical components used for buffering are costlier, hence a new class of algorithms are required to be developed for routing.

1.5.3 Performance Parameters

All the performance parameters described in section 1 4 2 are valid for All-Optical Switches but at the same time one more parameter is required which takes into account the effect of noise. Active components like Semiconductor Optical Amplifier or Fiber Amplifiers introduce different noises (i.e. ASE noise and Crosstalk noise) in the system These noises affect the Bit Error Rate at the receiver.

1.6 Optical Switch Architectures

Various switch architectures have been proposed in literature which can function as elementary switch module [3].

1.6.1 Fiber Delay Line Switch Architecture

The fiber delay line switch [3] is based on calibrated optical fiber delay lines, adjusted to multiples of packet duration.

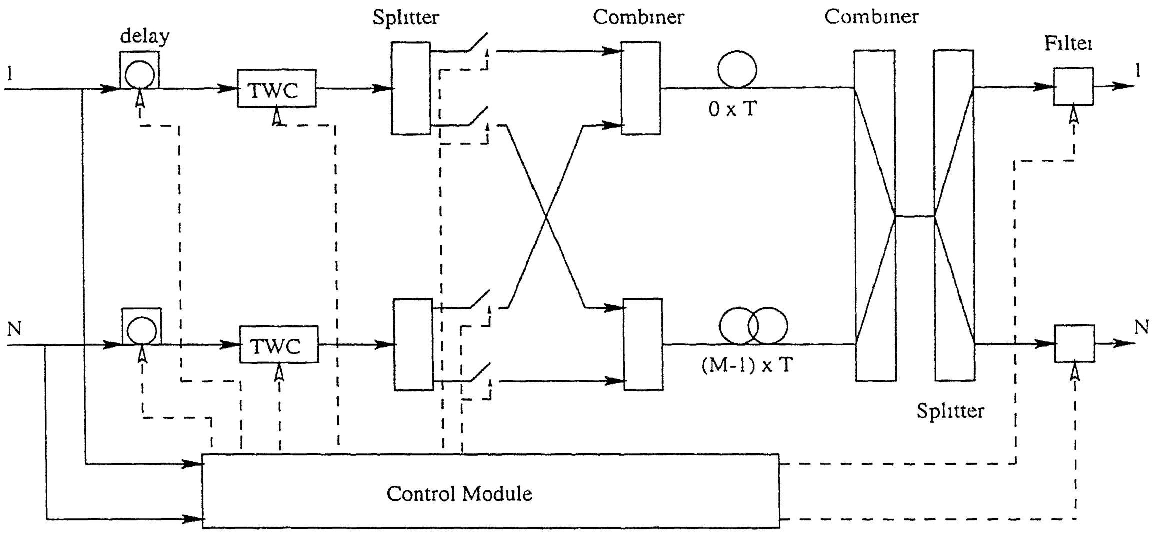

Figure 1.4: Fiber delay line Switch Matrix

Fig 1.4 shows the N input, N output switch module. It consists of N tunable optical wavelength converters that assign to each packet the wavelength corresponding to its target output, $N \times M$ optical gates providing to each tunable wavelength converter access to all fiber delay lines, M calibrated fiber delay lines with diferent delays, N bandpass filters at the output each tuned to a different wavelength thus defining the output address and some star couplers.

The control module drives all the components and manages the delay lines according to the switching algorithm.

1.6.2 Multidimensional Switch Architecture

This architecture exploits the wavelength domain (with wavelength converters) and space domain (with space switches) for contention resolution to minimize the amount of optical buffers required in a multistage switch arrangement [3]. The switch is shown in Fig 1.5

In case of contention, the packets competing for same output are converted to

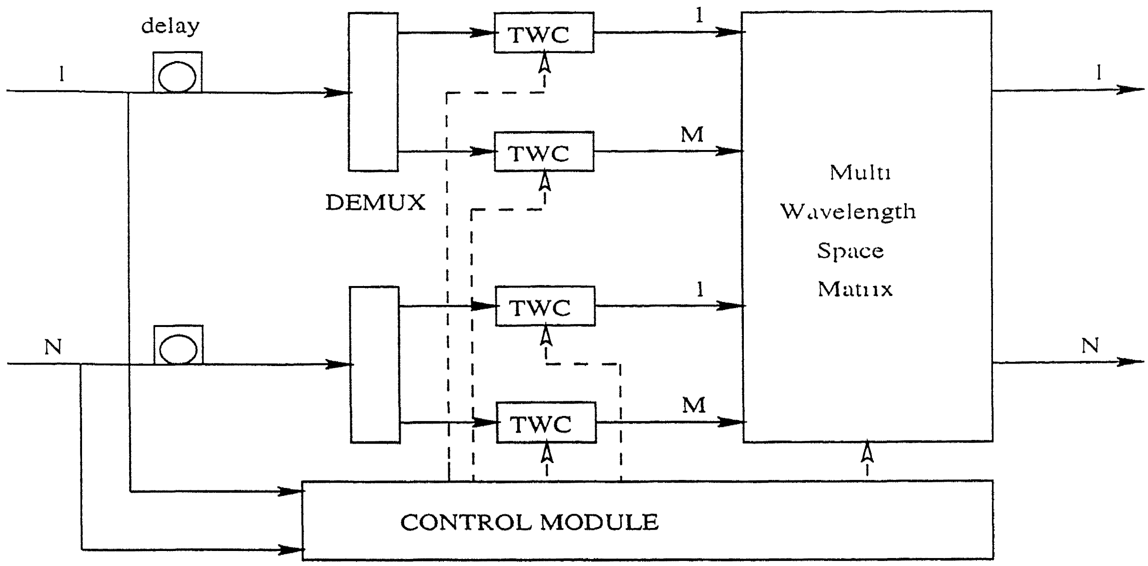

Figure 1 5: Multidimensional Switching Matrix

different wavelengths and transmitted at the same time slot instead of being delayed in a buffer and then transmitted consecutively.

1.6.3 Fiber Loop Buffer Memory Switch Architecture

The switch architecture [3] is shown in Fig. 1.6 The fiber loop length is equal to one packet period and the capacity of memory corresponds to a set of optical wavelengths to which the input packets are converted before being stored in the loop. The operation is assumed to be synchronous on packet period basis. In case of contention, the input ackets are converted to the available wavelengths in the loop and are kept circulating the WDM loop memory by activating the corresponding Semiconductor Optical plifier. In this work Fiber Loop Buffer Memory architecture has been analysed. hitecure has been treated in detail in chapter 3

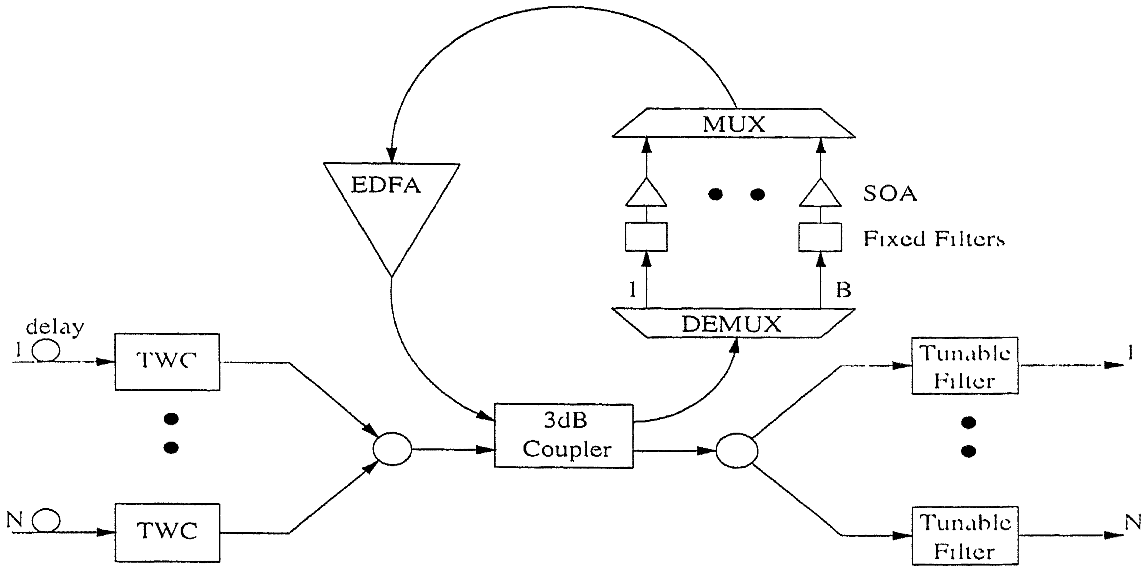

Figure 1.6: Fiber Loop Buffer Memory Architecture

1.7 Objective of the Thesis

Large size matrix fabrication is very difficult since physical limitations of current optical and optoelectronic devices introduce implementation constraints thus limiting the practical size of switch matrix. Therefore multistage matrices have to be realized by interconnecting elementary switch modules of limited size.

In this work Fiber Loop Buffer Memory has been analysed as Elementary Switch Module. The number of wavelengths put inside the loop determines the maximum buffer capacity but there is a limitation on this. With FLBM another parameter of interest is the limit on the number of recirculations allowed for a packet in the loop Because of the ASE noise introduced by SOA and EDFA in the loop it is not possible to allow the packets to stay in the loop for arbitrary amount of time. These parameters can only be determined on the basis of power budget consideration.

To decide about the limitations on these parameters a receiver has been introduced at the output of the switch. On the basis of Bit Error Rate at the receiver, limitations

on above parameters have been obtained. Various noises at the receiver including the beat noises due to interaction between signal and various noises need to be considered in this analysis.

1.8 Organization of Thesis

Chapter 2 deals with the description and modelling of various components, involved in Fiber Loop Buffer Memory (FLBM). Separate models have been used for Semiconductor Optical Amplifier and Erbium Dopped Fiber Amplifier. Receiver model is also given with the description of various noises Chapter 3 describes the full functioning of FLBM switch and effect of various parameters on the performance of the switch Chapter 4 gives results and discussion. Conclusions are given in chapter 5

Chapter 2

COMPONENT MODELLING

This chapter discusses key components and their modellings involved in the Fiber Loop Buffer Memory switch architecture. At the very beginning, most important components are described i.e. Semiconductor Optical Amplifier and Erbium Doped Fiber Amplifier These are the components which introduce most of the noise in optical systems therefore their analysis becomes very important.

2.1 Semiconductor Optical Amplifier

2.1.1 Description

In a physical system, atoms are found in one of possible discrete energy states. At thermal equilibrium atoms are said to be in their ground state. These atoms when absorb some energy attain high energy states. These high energy states are called excited states. These atoms return to their ground state by emitting some energy, equal to the difference of ground and excited state energy levels, in the form of radiation. The frequency of the emitted radiation depends on the difference of energy levels and

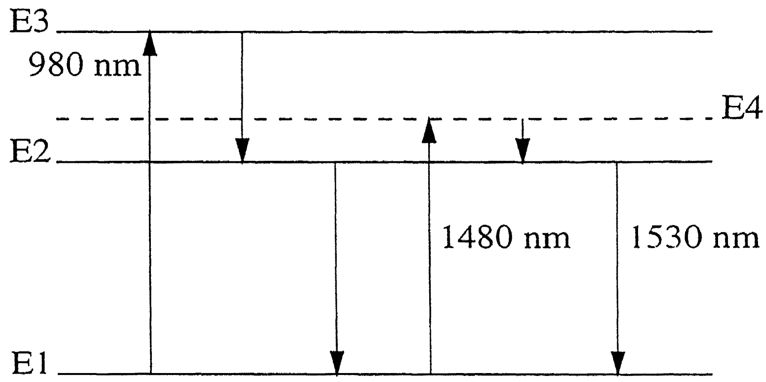

Figure 2.1: Energy Diagram

is given as :

$$E_2 - E_1 = h\nu \tag{2.1}$$

where E_2 is energy of higher state, E_1 is energy of lower state, h is Plank's constant and ν is the frequency of emitted radiation. The transition of atoms from higher energy state to lower energy state may be stimulated or spontaneous.

2.1.1.1 Spontaneous Emission

Independent of any external radiation, atoms in the higher state return to their ground state by emitting a photon. This is called as spontaneous emission. The emitted photons have same energy but they propogate in different directions with different phase and polarization. Thus spontaneously emitted light is incoherent in nature

2.1.1.2 Stimulated Emission

When a photon of frequency corresponding to the energy difference of higher and lower energy levels is incident on excited state atoms, it results in the emission of photons in same propagation direction, of same phase and polarization as that of stimulating photon. Thus the incident radiation gets amplified and the output radiation is coherent

nature

The amplification depends on the number of atoms in two states and requires more nber of atoms in higher state. This condition is called Population Inversion This dition is achieved by supplying additional energy to maintain higher number of ms in higher energy state. This process is called Pumping and can be done in ctrical (as in SOA) or in Optical (as in EDFA) form.

.2 Noise in SOA

re are mainly two types of noise present in SOA :

ASE Noise : Along with the desired radiation some radiation due to the spontaneous emission also takes place. This also gets amplified in the active region in addition to the incident signal. This is pure noise and some times may cause saturation of SOA.

Crosstalk . In the presence of a WDM signal at the input of SOA, signal at one wavelength deplete the carrier density so that other wavelengths see reduced population inversion and hence gain, thus other signal will not get amplified to the same extent. This is called as gain saturation crosstalk which is the reason why SOA's cannot be used for amplification of WDM signals.

Modelling

of SOA depends on the input power. The simple equation is given as [12]

$$G = G_0 exp\left(-\frac{(G-1)P_{in}}{P_{sat}}\right) \tag{2.2}$$

P_{in} = Input power to SOA,

P_{sat} = SOA Saturation Power Level,

and

G_0 = Unsaturated Gain of SOA.

The time constant for the gain variation is very small and is of the order of nano seconds therefore gain of SOA is different for bit "1" and bit "0". The signal is assumed to be intensity modulated with powers p_1 and p_0 for bit "1" and bit "0" where p_1 is fixed power while p_0 is zero. In the loop, noise is added to the signal so net power for bits is not constant. Let,

p_1^k be the average signal power for bit "1" after k^{th} rotation,

p_0^k be the average signal power for bit "0" after k^{th} rotation,

n_1^k be the average noise power for bit "1" after k^{th} rotation, and

n_0^k be the average noise power for bit "0" after k^{th} rotation

Input power to SOA for bit "1" is $(p_1^k + n_1^k)$ and for bit "0" is $(p_0^k + n_0^k)$. Hence the gains for bit "1" and "0" in $(k+1)^{th}$ rotation are

$$G_1^{k+1} = G_0 exp\left(-\frac{(G_1^k - 1)(p_1^k + n_1^k)}{P_{sat}}\right), \tag{2.3}$$

and

$$G_0^{k+1} = G_0 exp\left(-\frac{(G_0^k - 1)(p_0^k + n_0^k)}{P_{sat}}\right) \tag{2.4}$$

ASE noise for SOA is given by

$$P_{ASE} = \eta_{sp}(G-1)h\nu\ \Delta\nu, \tag{2.5}$$

where

η_{sp} = Spontaneous Emission noise factor,

h = Plank's Constant,

ν = Frequency of signal, and

$\Delta\nu$ = Optical Bandwidth

Noise added to the signal in k^{th} rotation for bit "1" and "0" are n_{a1}^k and n_{a0}^k and are given by

$$n_{a1}^k = \eta_{sp}(G_1^k - 1)h\nu\ \Delta\nu \tag{2.6}$$

and

$$n_{a0}^k = \eta_{sp}(G_0^k - 1)h\nu\ \Delta\nu. \tag{2.7}$$

Total noise at the output of SOA for bit "1" and "0" in $(k+1)^{th}$ rotation are

$$n_{1o}^{k+1} = n_1^k G_1^{k+1} + n_{a1}^{k+1}, \tag{2.8}$$

and

$$n_{0o}^{k+1} = n_0^k G_0^{k+1} + n_{a0}^{k+1}. \tag{2.9}$$

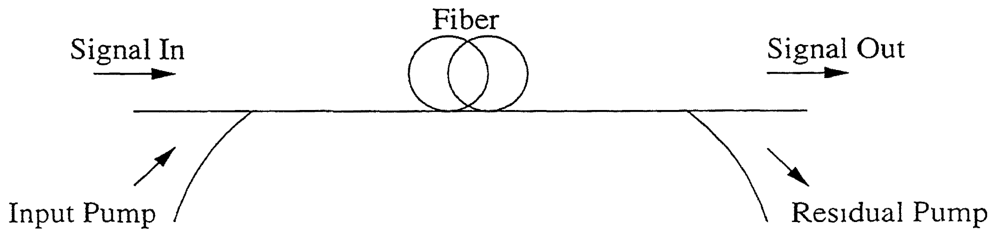

Figure 2 2: Erbium Doped Fiber Amplifier

2.2 Erbium Doped Fiber Amplifier

EDFA is basically a silica fiber whose core is dopped with Erbium ions (Er^{+3}), a rare earth element. Pumping is done in optical form by a separate Pump Laser. Wavelength selective couplers are used to couple the pump power into fiber and extract the residual power at the output (Fig. 2 2).

2.2.1 Description

The introduction of Erbium ions (Er^{+3}) produces a phenomenon called Stark Splitting, in which the higher energy level is splitted into multiple levels. The excited atoms have their electrons distributed in these splitted levels. Transition from these discrete levels to ground level corresponds to different wavelengths. These wavelengths fall in the low attenuation window of fibers(at 1 53 μm), for Er dopped fibers. There are several other advantages of EDFA over SOA,

- Crosstalk is very low for EDFA.
- Being an all fiber device, EDFA gain is independent of Polarization.
- Pump Lasers are readily available at 980/1480 nm which are suitable for EDFA pumping.
- EDFA is much simpler in construction and operation.

2.2.2 Noise in EDFA

EDFA is free from crosstalk but ASE noise is present. Along with ASE which has already been explained in the previous section, there is another source of noise, Excited State Emission (ESA) noise. Pump power is utilized in some unnecessary transitions, i.e. the atoms already in excited state may experience another upward transition. This reduces the pumping efficiency and limits the amplifier performance.

2.2.3 Modelling of Gain

Gain of EDFA is modelled as in [5]. Two level system is assumed with an arbitrary number of input beams. The rate equation for fractional population of higher state is given as

$$\frac{\partial N_2(z,t)}{\partial t} = -\frac{N_2(z,t)}{\tau} - \frac{1}{\rho A}\sum_{j=1}^{N} u_j \frac{\partial P_j(z,t)}{\partial z}, \tag{2.10}$$

where

$P_k(z,t)$ = Power at wavelength λ_k as a function of distance and time,

$N_1(z,t)$ = Fractional Population of the lower state,

$N_2(z,t)$ = Fractional Population of the higher state,

such that

$$N_1(z,t) + N_2(z,t) = 1, \tag{2.11}$$

N = Number of beams of wavelength λ_k,

L = Length of EDFA,

ρ = Density of active atoms,

A = Cross sectional area of active volume,

u_k = Direction of propagation of beams, and

τ = Spontaneous life time of higher level.

u_k is +1 if the beam enters at $z = 0$ and exits from $z = L$ If beam travels in reverse direction, u_k = -1

Change of power in k^{th} beam is described by

$$\frac{\partial P_k(z,t)}{\partial t} = \rho u_k \Gamma_k [(\sigma_k^e + \sigma_k^a) N_2(z,t) - \sigma_k^a] P_k(z,t), \tag{2 12}$$

where

σ_k^e , σ_k^a = Cross sections for stimulated emission and absorption at wavelength λ_k and

Γ_k = Confinement factor of fiber amplifier at wavelength λ_k.

Under steady state condition

$$\frac{\partial N_2(z,t)}{\partial t} = 0, \tag{2 13}$$

hence we can write

$$\frac{u_k}{P_k(z)} dP_k = -[\alpha_k + \frac{1}{P_k^{IS}} \sum_{j=1}^{N} u_j \frac{dP_j(z,t)}{dz}]\, dz, \tag{2 14}$$

where

α_k = Absorption Constant, and

P_k^{IS} = Intrinsic Saturation Constant.

In the above α_k and P_k^{IS} are given by

$$\alpha_k = \rho \Gamma_k \sigma_k^a, \tag{2.15}$$

and

$$P_k^{IS} = \frac{A}{\Gamma_k(\sigma_k^e + \sigma_k^a)\tau}. \tag{2.16}$$

Finally integrating Eqn.(2 14) gives

$$P_k^{out} = P_k^{in} exp(-\alpha_k L) exp\left(\frac{(P_{in} - P_{out})}{P_k^{IS}}\right). \tag{2 17}$$

where

P_k^{in} = Input power for the k^{th} beam, and

P_k^{out} = Output power for the k^{th} beam.

P_{in} and P_{out} are total input and output powers and are given as

$$P_{in} = \sum_{j=1}^{N} P_j^{in}, \tag{2 18}$$

and

$$P_{out} = \sum_{j=1}^{N} P_j^{out}. \tag{2.19}$$

Hence,

$$P_{out} = \sum_{j=1}^{N} A_k exp(-B_k P_{out}), \tag{2 20}$$

where

$$A_k = P_k^{in} exp(-\alpha_k L) exp\left(\frac{P_{in}}{P_k^{IS}}\right) \tag{2 21}$$

and

$$B_k = \frac{1}{P_k^{IS}}. \tag{2 22}$$

Since A_k and B_k are known constants if α_k , P_k^{IS} and the input powers are known, above equations can be solved for P_{out} . Once solved this can be put in Eqn.(2.17) to compute directly the output power P_k^{out} at each wavelength. In the above analysis P_j^{in} and P_j^{out} are time averaged powers.

ASE noise for EDFA for a wavelength λ_k is given as

$$P_k^{ASE} = \eta_{sp}(G_k - 1)\ h\nu_k\ \Delta\nu, \tag{2 23}$$

where

η_{sp} = Spontaneous Emission factor of EDFA,

ν_k = Frequency of k_{th} beam, and

$\Delta\nu$ = Opical Bandwidth at any wavelength.

2.3 Coupler and Splitter

A 2X2 coupler or splitter is a four port device as shown in Fig. 2.3. It has two input and two output ports. Power of input port 1 is divided in two parts such that a fraction α goes through port 3 while other fraction goes to port 4. Similarly power at input

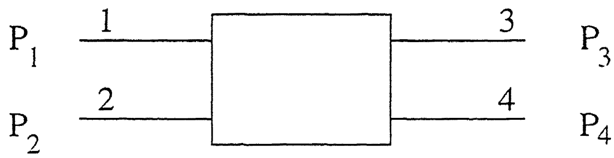

Figure 2.3: 2X2 Coupler or Splitter

2 is divided such that the α fraction goes to port 4 while other fraction go to port 3 Assuming power at port 2 as zero, Splitting Loss is defined as

$$\alpha = 10 \, log_{10} \frac{P_4}{P_3 + P_4} \; dB \tag{2.24}$$

Excess Loss is defined as

$$excess \; loss = 10 \, log_{10} \frac{P_1}{P_3 + P_4} \; dB \tag{2.25}$$

Insertion Loss is defined as sum of excess loss and splitting loss, i.e.

$$Insertion \;\; Loss = splitting \; loss \; + \; excess \; loss, \tag{2.26}$$

$$Insertion \;\; Loss = 10 \, log_{10} \, \frac{P_1}{P_4} \; dB \tag{2.27}$$

All these losses have been assumed to be same for both ports

2.4 Multiplexer and Demultiplexer

Multiplexers and Demultiplexers are realized by connecting 2×2 couplers in succession [10] The realizations are shown in Fig. 2.4 and 2.5.

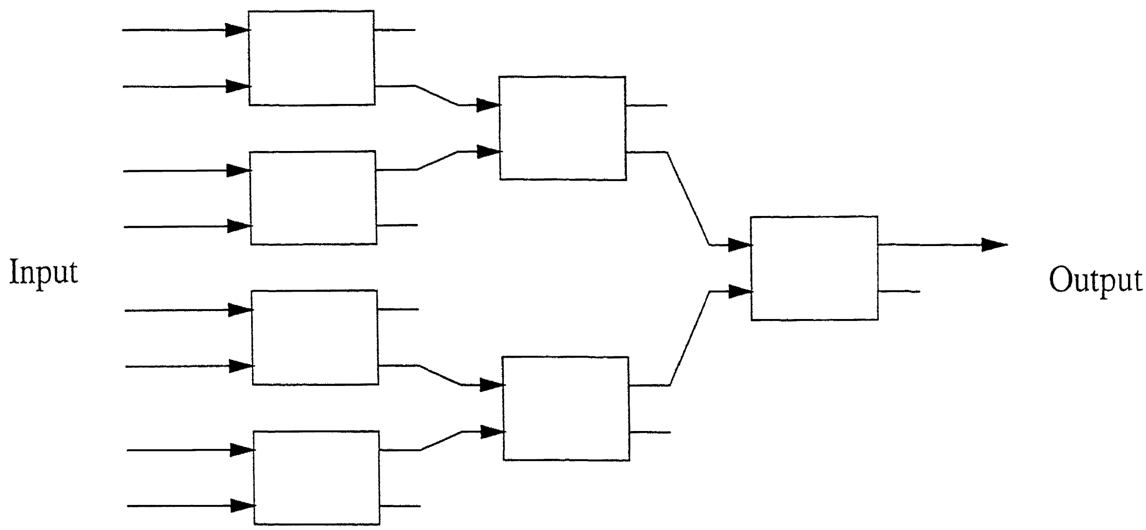

Figure 2.4: Multiplexer Realization

When number of inputs (or outputs for DEMUX) is up to two, single stage realization is required, when it is between 2 and 4, two stage realization is required and so on, therefore it can be shown that the loss for each channel is

$$Loss_{mux} = \lceil log_2\, M \rceil\; \beta,^{1} \tag{2.28}$$

where

β = Insertion Loss for a single coupler, and

M = Total number of inputs (or outputs for DEMUX)

Demultiplexer is essentially reverse of multiplexer with filter at every output. The loss is given as

$$Loss_{demux} = \lceil log_2 M \rceil \beta + L_f, \tag{2.29}$$

where

L_f = Filter Loss.

It is assumed that filters are ideal hence $L_f = 0$.

[1] $\lceil x \rceil$ means, smallest integer which is greater than or equal to real number x

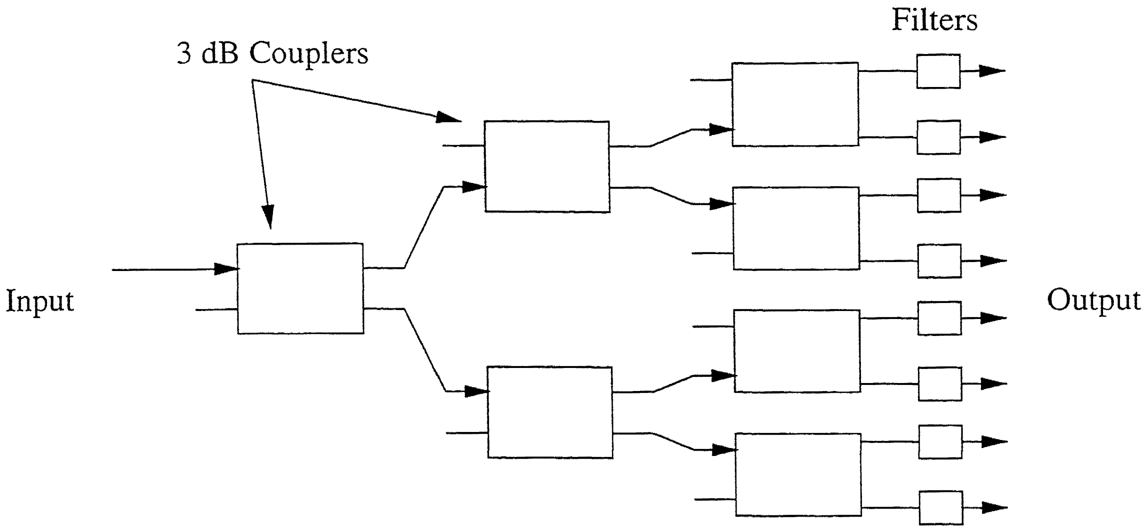

Figure 2.5: Demultiplexer Realization

2.5 Tunable Wavelength Converters

Wavelength Converter is a device that converts data from one incoming wavelength to another outgoing wavelength. There are three fundamental ways of achieving wavelength conversion, [11] optoelectronic method, optical gating method and wave mixing method. The first method is conversion of optical signal to electrical one and then modulating it over another wavelength. The second method is most suitable for Intensity Modulated signals and is defined in the next section. The last method uses the concept of Four Wave Mixing in SOA.

2.5.1 Optical Gating Method

This method makes use of an optical device whose characteristics change with the intensity of an input signal. The change is then transferred to another unmodulated probe signal at a different wavelength. Nonlinear effects of SOA can be used in two ways to make a wavelength converter.

- Cross-Gain Modulation . SOA gain depends on the input power. As the input power increases the gain decreases, if a low power prob signal at a different wavelength is sent in to SOA, it will experience low gain when bit "1" is transmitted as the input signal, and will experience high gain when bit "0" is transmitted Although simple, the extinction ratio achievable in this method, is small.
- Cross-Phase Modulation : The carrier density in the amplifier varies with the input signal and produces change in refractive index. this in turn modulates the phase of the probe signal. This phase change can be converted to intensity modulation by using an interferometer

2.6 Receiver Model

Receivers can be classified in two categories, Anolog Receiver and Digital Receivers [9] For Anolog Receivers the performance is measured in terms of minimum SNR required at the receiver input. Similarly for Digital Receivers the parameter is the Bit Error Rate. In this work Digital Receivers have been considered.

The signal is assumed to be intensity modulated digital signal and the receiver incorporated is of Direct Detection type. Direct Detection receiver is essentially a photodiode plus an amplifier with possibly additional signal processing circuits The optical signal is converted to electrical signal by photodiode which is then amplified by an electrical amplifier before further processing can take place The input optical power required at the receiver is a function of detector combined with electrical components within the receiver.

2.6.1 Various Noises in Receiver

There are variety of noises present in the receiver. They are as described below [6,7]

- Thermal Noise : Thermal interaction between free electrons and the vibrating atoms in any conducting medium produces spontaneous fluctuations in the current. This is especially prevalent in resistors at room temperature. The thermal noise current in a resistor R_L can be modelled as Gaussian random process with zero mean in the receiver bandwidth and variance of this noise current is given as

$$\sigma_{th}^2 = \frac{4KTB_e}{R_L}, \tag{2.30}$$

where

K = Boltzman Constant,

T = Temperature in Kelvin,

B_e = Electrical Bandwidth of Receiver, and

R_L = Load Resistance.

- Shot Noise : Due to the random distribution of electrons generated even when the incident optical power is constant, a small noise current is produced. This current can be modelled as Gaussian random process with mean as the constant current while the variance is given as

$$\sigma_{sh}^2 = 2eIB_e, \tag{2.31}$$

where

e = Electronic Charge, and

I = Constant current due to incident signal power.

- Beat Noise . The photo detector produces a current that is proportional to the optical power. The optical power is proportional to the square of the electric field. Thus the ASE noise field beats with the signal and itself, giving rise to beat noise components. Various beat noises present in the receiver and the variances of the corresponding noise currents are

- Signal-Spontaneous beat noise

$$\sigma^2_{sig-sp} = \frac{2R^2 B_e P_s P_{sp}}{B_o}, \tag{2.32}$$

- Spontaneous-Spontaneous beat noise

$$\sigma^2_{sp-sp} = \frac{(RP_{sp})^2 B_e (2B_o - B_e)}{B_o^2}, \tag{2.33}$$

and

- Spontaneous-Shot beat noise

$$\sigma^2_{sp-sh} = 2ReB_e P_{sp}, \tag{2.34}$$

where

R = Responsivity,

B_e = Electrical Bandwidth of the Receiver,

B_o = Optical Bandwidth,

P_s = Received Signal Power at the Receiver, and

P_{sp} = ASE Noise Power Received at the Receiver.

2.6.2 BER

Bit Error Rate for Direct Detection Receiver is given as [11]

$$BER = \frac{1}{2}\, erfc\left[\frac{I_1 - I_0}{\sqrt{2}(\sigma_1 + \sigma_0)}\right], \tag{2.35}$$

where

I_1 = Constant Current due to Received Power when bit "1" is transmitted,

I_0 = Constant Current due to Received Power when bit "0" is transmitted,

σ_1 = Variance of sum of all the Noise Currents when bit "1" is transmitted, and

σ_0 = Variance of sum of all the Noise Currents when bit "0" is transmitted

Chapter 3

FIBER LOOP BUFFER MEMORY NOISE ANALYSIS

3.1 Functioning of FLBM

The detailed diagram of FLBM switch is shown in Fig. 3.1. TWC's at the input of switch fabric converts the wavelength of an incoming packet to any one of the wavelengths supported by the switch. At the desired output line, the Tunable Filter is set to the same wavelength to select the packets. This way a packet is routed from input to output in the same time slot.

The selection of wavelengths at TWC's and TF's are done by the control module which does this according to header of the incoming packet The header of the packet is processed before the packet reaches to TWC's input. The control module is electronic hence the header part of packet is converted to electrical form which is then processed at the control module. In this work only switch module is considered.

In case of contention, one of the packets contending for same output line is allowed

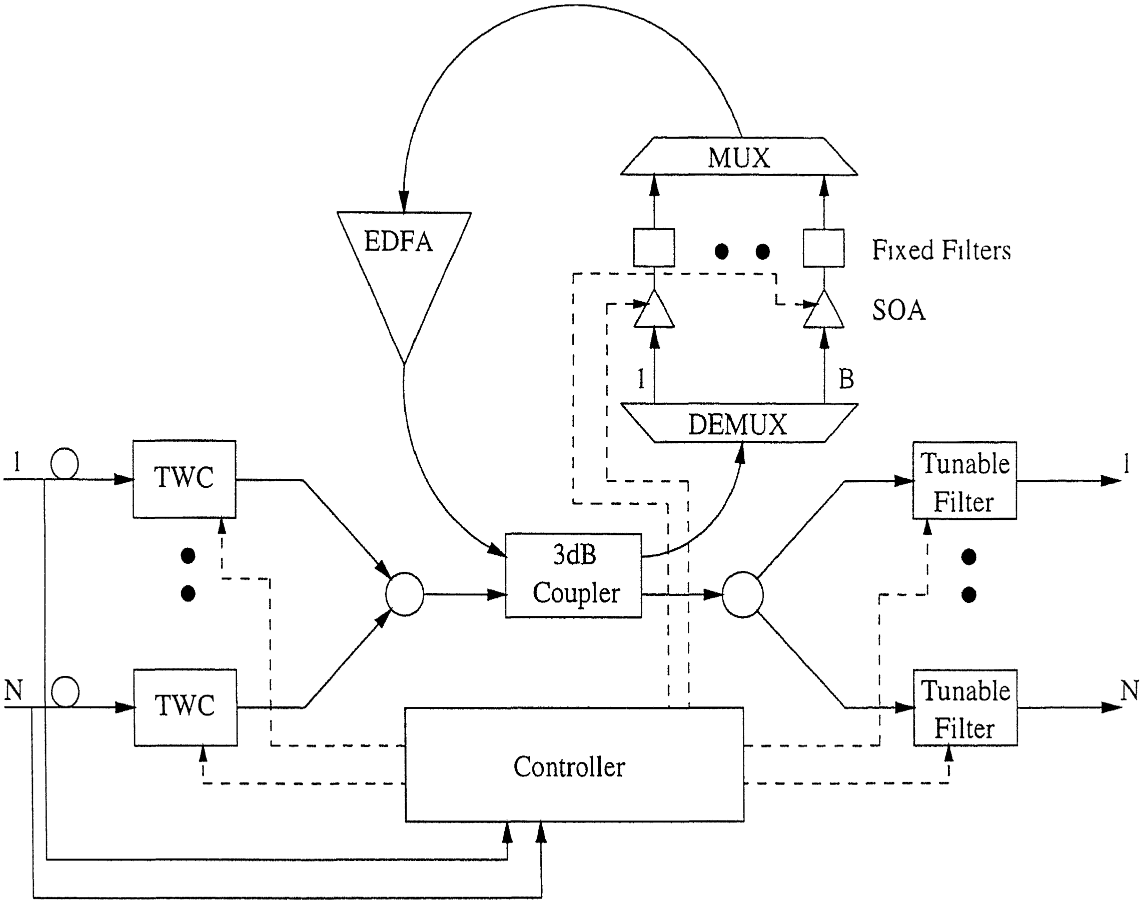

Figure 3 1: Fiber Loop Buffer Memory

to pass while others are stored on different wavelengths. The SOA's corresponding to these wavelength are turned "ON" and others are kept "OFF" The length of fiber in the loop plus the EDFA length introduces a delay of one time slot to the packet and they reach 3dB coupler input at the begining of next slot. This signal is mixed with signals coming from the input sides in the next slot and processed further If packets are again in contention corresponding SOA's continue to be "ON" and if contention is resolved the SOA's are turned "OFF" to erase the packet from the loop. This way packets are stored and forwarded by the switch. Control Module sends control signals to all devices to set them appropriately in the loop according to routing algorithm.

3.2 Need of EDFA

The SOA in the loop, basically functions as an ON/OFF switch but it additionally provides some gain also. Without EDFA, SOA is the only gain providing element in the loop, all other elements account for attenuation only The attenuation in loop largely comes from the Demultiplexer and Multiplexer and for a given number of wavelenghts in the loop, is same for both. The gain of SOA is not very large and hence if the number of wavelengths in loop is more, the total loss in loop becomes larger than SOA gain and the signal gets attenuated rapidly with number of rotations Hence EDFA is needed to support more number of wavelengths in loop. EDFA is used to amplify WDM signals hence it amplifies all packets in the loop and thus a single EDFA is needed in the loop

3.3 Recirculation Limit

The analytical models for various components including SOA, and EDFA were presented in the last chapter. The models fully describe the input - output signal relations for all the components. With the help of these models analytical expressions have

been obtained which are useful for the computation of signal and noise power for bit "1" and "0" after every recirculation. Inside the loop the signal and noise experience, attenuation due to Multiplexer, Demultiplexer and 3dB coupler and gain due to SOA and EDFA SOA and EDFA also introduce amplified spontaneous noise (ASE) in every rotation

The signal and noise power levels inside the loop depends on the number of recirculations, completed by signal in the loop. This is mainly because of the gain saturation in SOA and EDFA. Gain of SOA depends on power level at its input and thus varies with power The ASE noise introduced by SOA is also a function of Gain and thus varies with power at input of SOA. Similarly the gain and ASE noise for EDFA also depends on the input power levels, the only difference is that SOA amplifies a single wavelength signal while EDFA amplifies multiple wavelength multiplexed signals. Thus the gain and the noise generated by EDFA for any wavelength depends not just on that wavelength but also on the signals on other wavelengths.

Therefore the noise analysis in loop is highly dependent on the the number of packets present in the loop at any time. The analysis of the switch has been done by considering the load on the switch. A simulation has been performed to determine the average number of packets in the loop for different *Packet Arrival Rates* for uniform load conditions in the switch. A simple routing scheme has been considered for the simulation work and is described in the last section.

The Bit Error Rate is determined by the signal and noise powers for bit "1" and "0" at the switch output for one channel. Various noises (i.e. thermal noise, shot noise, beat noises etc.) appearing in the receiver also play vital role in determining the Bit Error Rate Thus Bit Error Rate at the receiver depends on the number of rotations made by the signal before reaching to the receiver. As the number of rotations in the loop increase, Bit Error Rate performance at the receiver degrades, thus limiting the maximum number of recirculations made by a packet in the loop This recirculation

limit has been determined by varying various parameters of the switch like, the size of the switch, the maximum number of wavelengths available in the loop, input power to the switch etc

3.4 Loop Model

3.4.1 Notation

Subscript "k" whereever used is for wavelength λ_k while "j" is for number of rotations already completed.

Let,

$p_0^{k,in}$, $n_0^{k,in}$, $p_1^{k,in}$, $n_1^{k,in}$ are the signal and noise powers for bit "0" and "1" at the input of the switch for wavelength λ_k. n_0^{in}, n_1^{in} and p_0^{in} are assumed to be zero at the switch input.

$p_0^{j,k,out}$, $n_0^{j,k,out}$, $p_1^{j,k,out}$, $n_1^{j,k,out}$ are the signal and noise powers for bit "0" and "1" at the output of the switch for wavelength λ_k after the signal has completed j rotations in loop.

$G_{soa,1}^{j,k}$, $G_{soa,0}^{j,k}$ are Gain of SOA for bits "1" and "0" when the signal on a wavelength λ_k has already completed j rotations in loop.

$G_{edfa}^{j,k}$ is Gain of EDFA for a packet when the signal on wavelength λ_k has already completed j rotations in loop.

$P_{1,edfa}^{j,k,in}$, $P_{0,edfa}^{j,k,in}$ are Signal Power on wavelength λ_k for bit "1" and "0" at the input of EDFA, when it has already completed j rotations in loop

$P_{1,edfa}^{j,k,out}$, $P_{0,edfa}^{j,k,out}$ are Signal Power on wavelength λ_k for bit "1" and "0" at the output

of EDFA, when it has already completed j rotations in loop

$n_{1,edfa}^{j,k,in}$, $n_{0,edfa}^{j,k,in}$ are Noise Power on wavelength λ_k for bits "1" and "0" at the input of EDFA, when it has already completed j rotations in loop.

$n_{1,edfa}^{j,k,out}$, $n_{0,edfa}^{j,k,out}$ are Noise Power on wavelength λ_k for bits "1" and "0" at the output of EDFA, when it has already completed j rotations in loop

$p_{avg}^{j,k,in}$, $p_{avg}^{j,k,out}$ are Average Signal Power on wavelength λ_k at input and output of EDFA when the signal has already completed j rotations in loop

$n_{avg}^{j,k,in}$, $n_{avg}^{j,k,out}$ are Average Noise Power on wavelength λ_k at input and output of EDFA when the signal has already completed j rotations in loop.

$n_{a1,soa}^{j,k}$ and $n_{a0,soa}^{j,k}$ are the ASE noise which gets added to bits "1" and "0" in $(j+1)^{st}$ rotation $n_{a,edfa}^{j,k}$ is the ASE noise added due to EDFA in $(j+1)^{st}$ rotation

Also,

$$p_{avg}^{j,k,in} = \frac{p_{1,edfa}^{j,k,in} + p_{0,edfa}^{j,k,in}}{2}, \tag{3.1}$$

and

$$n_{avg}^{j,k,in} = \frac{n_{1,edfa}^{j,k,in} + n_{0,edfa}^{j,k,in}}{2}. \tag{3.2}$$

3.4.2 Power equations for EDFA

Average output power at the output of EDFA for k^{th} channel, when the signal has completed j rotations in the loop is given by

$$p_{avg}^{j,k,out} = p_{avg}^{j,k,in} G_{edfa}^{j,k} \tag{3.3}$$

Also the noise at the output of EDFA for k^{th} channel, when the signal has completed j rotations in the loop is given by

$$n_{avg}^{j,k,out} = n_{avg}^{j,k,in} G_{edfa}^{j,k} + n_{a,edfa}^{j,k}. \tag{3.4}$$

3.4.3 Power equations at the output of switch

When a packet is not in contention it straight away goes to output without entering the loop, hence bit powers at the output after 0 circulations are given as

$$p_1^{0,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})^2} p_1^{k,in}, \tag{3.5}$$

$$p_0^{0,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})^2} p_0^{k,in}, \tag{3.6}$$

$$n_1^{0,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})^2} n_1^{k,in}, \tag{3.7}$$

and

$$n_0^{0,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})^2} n_0^{k,in}. \tag{3.8}$$

Bit powers at the output of switch when the signal has completed j rotations in the loop can be given, in terms of bit powers at the output of EDFA as

$$p_1^{j,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})} p_{1,edfa}^{(j-1),k,out}, \tag{3.9}$$

and

$$p_0^{j,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})} p_{0,edfa}^{(j-1),k,out} \quad (3\ 10)$$

Similarly, the noise power at the output of switch are given by

$$n_1^{j,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})} n_{1,edfa}^{(j-1),k,out}, \quad (3\ 11)$$

and

$$n_0^{j,k,out} = \frac{1}{2(2^{\lceil log_2 N \rceil})} n_{0,edfa}^{(j-1),k,out} \quad (3\ 12)$$

3.4.4 Power equations at the input of EDFA

When a packet first time enters the loop, bit and noise powers at the input of EDFA in terms of input bit powers are given as

$$p_{1,edfa}^{0,k,in} = \frac{1}{2(2^{\lceil log_2 N \rceil})(2^{\lceil log_2 B \rceil})^2} G_{soa,1}^{0,k} p_1^{k,in}, \quad (3.13)$$

$$p_{0,edfa}^{0,k,in} = \frac{1}{2(2^{\lceil log_2 N \rceil})(2^{\lceil log_2 B \rceil})^2} G_{soa,0}^{0,k} p_0^{k,in}, \quad (3\ 14)$$

$$n_{1,edfa}^{0,k,in} = \frac{1}{2(2^{\lceil log_2 N \rceil})(2^{\lceil log_2 B \rceil})^2} G_{soa,1}^{0,k} n_1^{k,in} + \frac{n_{a1,soa}^{0,k}}{(2^{\lceil log_2 B \rceil})}, \quad (3.15)$$

and

$$n_{0,edfa}^{0,k,in} = \frac{1}{2(2^{\lceil log_2 N \rceil})(2^{\lceil log_2 B \rceil})^2} G_{soa,0}^{0,k} n_0^{k,in} + \frac{n_{a0,soa}^{0,k}}{(2^{\lceil log_2 B \rceil})}. \tag{3 16}$$

When the packet enter the loop after completing j rotations, the signal and noise powers at the input of EDFA are given as

$$p_{1,edfa}^{j,k,in} = \frac{1}{2(2^{\lceil log_2 B \rceil})^2} G_{soa,1}^{j,k} p_{1,edfa}^{(j-1),k,out}, \tag{3.17}$$

$$p_{0,edfa}^{j,k,in} = \frac{1}{2(2^{\lceil log_2 B \rceil})^2} G_{soa,0}^{j,k} p_{0,edfa}^{(j-1),k,out}, \tag{3 18}$$

$$n_{1,edfa}^{j,k,in} = \frac{1}{2(2^{\lceil log_2 B \rceil})^2} G_{soa,1}^{j,k} n_{1,edfa}^{(j-1),k,out} + \frac{n_{a1,soa}^{j,k}}{(2^{\lceil log_2 B \rceil})}, \tag{3 19}$$

and

$$n_{0,edfa}^{j,k,in} = \frac{1}{2(2^{\lceil log_2 B \rceil})^2} G_{soa,0}^{j,k} n_{0,edfa}^{(j-1),k,out} + \frac{n_{a0,soa}^{j,k}}{(2^{\lceil log_2 B \rceil})}. \tag{3 20}$$

3.5 Simple Routing Scheme

This section describes characteristics of a simple routing scheme used for simulation, to find the average number of packets in loop under different loading conditions.

- Switch size is $N \times N$, therefore a maximum of N packets can arrive in any time slot at the switch input. All packets are assumed to be synchronized.
- B is the total number of wavelengths available in the loop and therefore is the total buffer capacity.

Chapter 4

Results and Analysis

In this chapter the results of performance analysis of the elementary switch based on Fiber Loop Buffer Memory are presented. The results are based on the computational model using different components in the loop described in chapter 2. This study focuses on the Bit Error Rate at the output of the switch architecture considered. Switches of different size are considered. Issue regarding the size of the switch are also investigated.

4.1 Size of Elementary Switch Module

Large size switch module fabrication is not feasible, therefore small size switches are fabricated and interconnected in cascade to build a large size switch. For FLBM switch when there is no contention, the signal passes through the switch without entering the loop. In this case it experiances a total attenuation of $1/2N^2$, where N is the size of the switch. For a 2×2 switch this loss is 1/8. If a large switch (say 8×8 as shown in Fig. 4.1) is constructed with multiple 2×2 switches, the total attenuation is greater than when it is constructed with a single FLBM switch. This is shown in Fig 4.1.

Using multiple 2×2 switches also requires a large number of components (i.e. SOAs

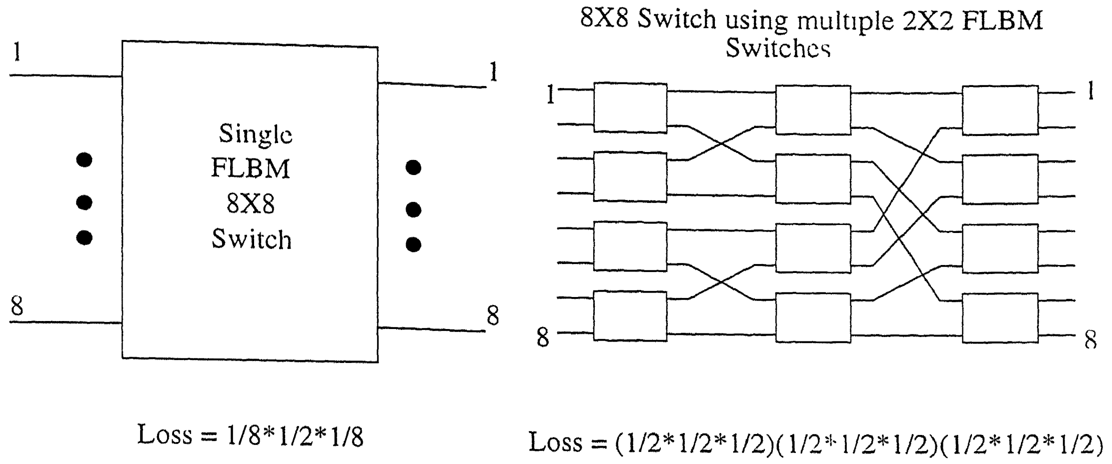

Figure 4.1. Loss for 8×8 switch for different types of construction

Filters EDFAs etc.) Therefore it is desirable to have an Elementary Switch Module of as large size as possible.

4.2 Some Parameters

In this section some parameters of switch are presented

4.2.1 Length of Fiber in the Loop

The length of fiber in the loop includes the length of the Erbium Dopped Fiber Amplifier. The total length corresponds to delay of one slot or one packet time. Thus calculation of length requires the knowledge of data rate as well as the packet size. The light travels through the fiber (of approximate effective refractive index 1.5) at a speed of 2×10^8 m/sec. Thus the length of fiber in loop is the distance light travels at a speed of 2×10^8 m/sec in one slot duration.

4.2.2 Wavelength Range

The wavelengths used are in the range of 1525 nm to 1590 nm The channels are separated by a channel spacing of 2 nm. Thus a total of 32 wavelengths are used for the analysis This is the range valid for the EDFA model considered here.

4.2.3 Specifications for SOA

With respect to the model of SOA described in section 2.2, the parameters of SOA used are the following.[10]

$$Unsaturated\ Gain,\ G_0 = 20\ dB$$

$$Saturated\ Power,\ P_{sat} = 1.55\ dBm$$

$$Spontaneous\ Emission\ Noise\ factor,\ \eta_{sp} = 1.5$$

4.2.4 Specifications for EDFA

Various parameters with respect to the model of EDFA presented in section 2 1 are the following.[5,8]

$$Level\,2\,to\,level\ 1\ transition\ time\ constant\ \tau = 0.01\ sec$$

$$Mode\ radius = 3.2 \times 10^{-6}\ m$$

$$Density\ of\ Erbium\ Atoms = 2.0 \times 10^{24}\ per\ m^3$$

$$Spontaneous\ Emission\ noise\ factor\ \eta_{sp} = 1.5$$

$$Pump\,power\ wavelength\ \lambda_p = 1480\ nm$$

$$Input\ pump\ power = 15\ mWatts$$

$$Length\ of\ EDFA = 15\ m$$

$$Confinement\ factor\ \Gamma_k = 0.36273292$$

$$Crosssection\ for\ stimulated\ emission\ \sigma_k^e = 8.1 \times 10^{-21} cm^2$$

$$Crosssection\ for\ absorption\ \sigma_k^a = 4.83 \times 10^{-21} cm^2$$

4.2.5 Specifications for Receiver

Various parameters with respect to the model of receiver presented in section 2.5 are the following.[6,7]

$$Electrical\ Bandwidth\ of\ Receiver = 1.25\ GHz$$

$$Optical\ Bandwidth\ of\ Receiver = 10\ GHz$$

$$Load\ Resistance = R_L$$

$$Quantum\ Efficiency\ of\ Photo\ Detector\ \eta = 1$$

4.3 Observations from simulation

Fig. 4 2 shows the variation in the number of packets present in the loop on an average for different load on the switch. The traffic arriving at the switch is assumed to be uniformaly distributed For lower loads the chances of contention are less hence the number of packets present in loop is also less. For higher loads the average number of packets in loop increases. It is seen that the average number of packets is always less than the total number of wavelengths

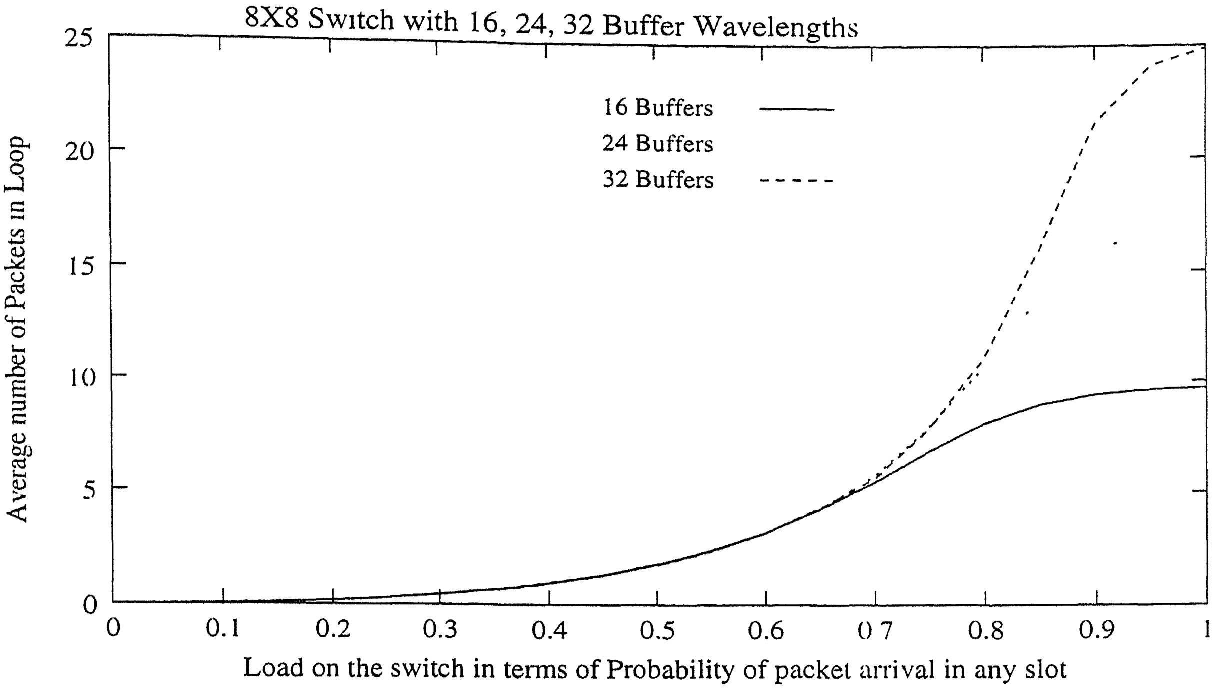

Figure 4 2: Average number of packets in loop for different Arrival Rates

Fig. 4.3 is a similar figure for 16×16 switch. Simulation results are shown for large number of wavelengths even when the results shown in following sections are limited to a maximum of 32 wavelengths in the loop. The flat region in the plots indicate the requirement of large number of buffer wavelengths in the loop for higher loads. This will further increase with the increase in size of switch. Therefore large size switch will require large number of wavelengths to support higher loads This requirement limits the size of Elementary Switch Module.

4.4 Observations for 8×8 switch

Three cases are considered for 8×8 switch. They are for 16, 24 and 32 number of total available wavelengths in the loop. For all cases, performance was observed under different loading conditions. For very small loads only one packet was considered in the loop on an average in the switch. Average number of packets in loop was obtained

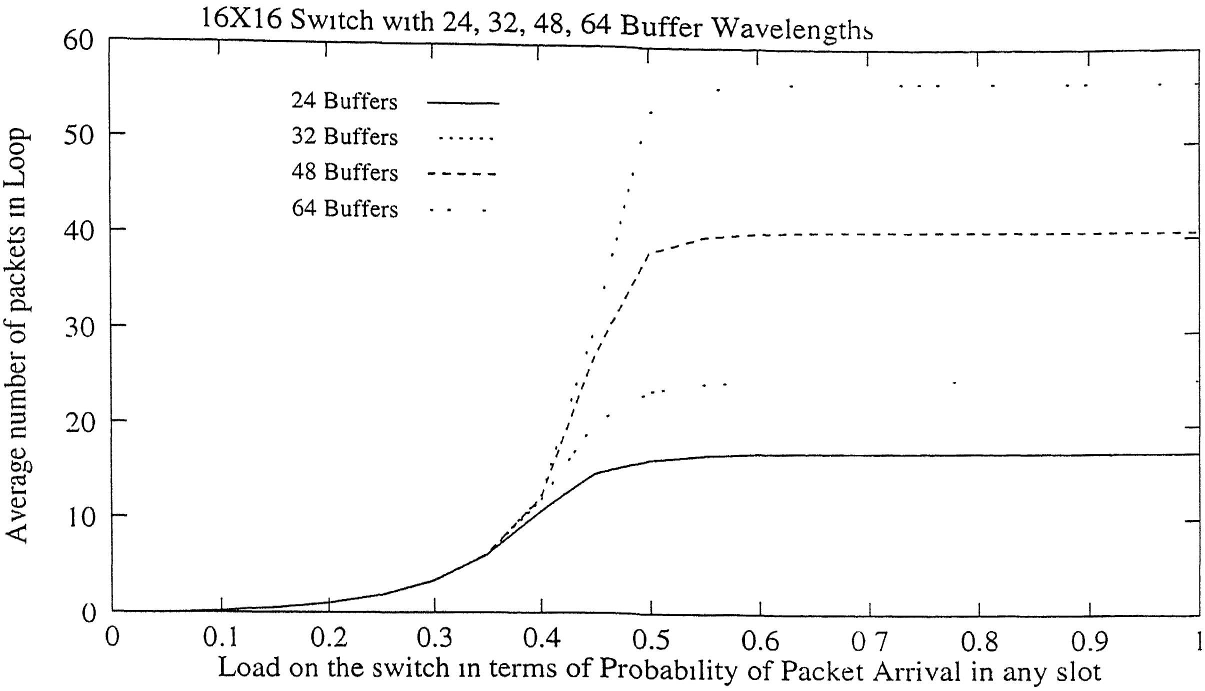

Figure 4.3. Average number of packets in loop for different Arrival Rates

from simulation for 0.85 Probability of Packet Arrival in any slot. The calculations are done for this case also Finally when there are packets on all the wavelengths that case is also considered. For all the three cases different plots are shown for different input powers. Fig. 4 4 shows BER performance on a single channel for various input powers, with number of recirculations in the loop when there is no other packet in loop.

Fig. 4 5 and Fig. 4.6 are similar plots when 9 and 16 packets are present in loop respectively Fig. 4.7 , 4.8 and 4.9 are for same switch with 24 buffer wavelengths and Fig. 4.10 , 4.11 and 4.12 are for 32 buffer wavelengths.

From these figures it is clear that performance in terms of recirculation limit, improves with increase in the average number of packets present in the loop It is also seen that with increase in input power the recirculation limit gets better.

This happens because the power level at the input of EDFA in the first circulation is very less and hence EDFA gain is very large. This large gain produces large ASE noise

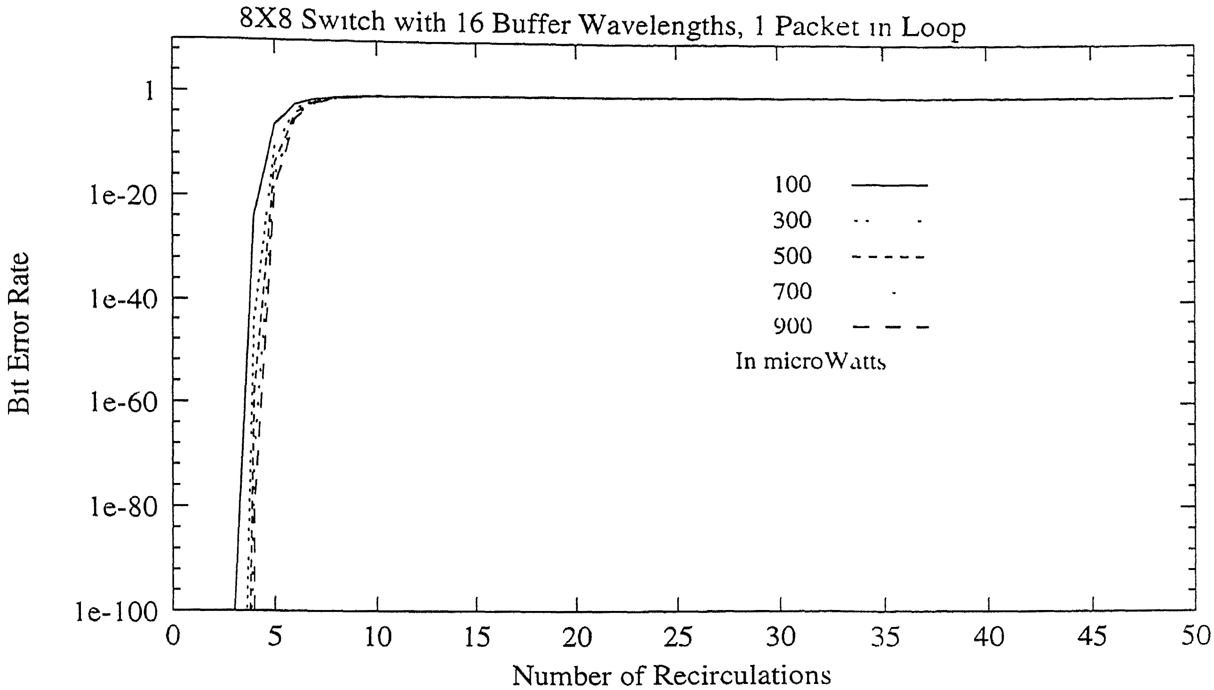

Figure 4.4. BER variation with number of recirculations for diff number of packets

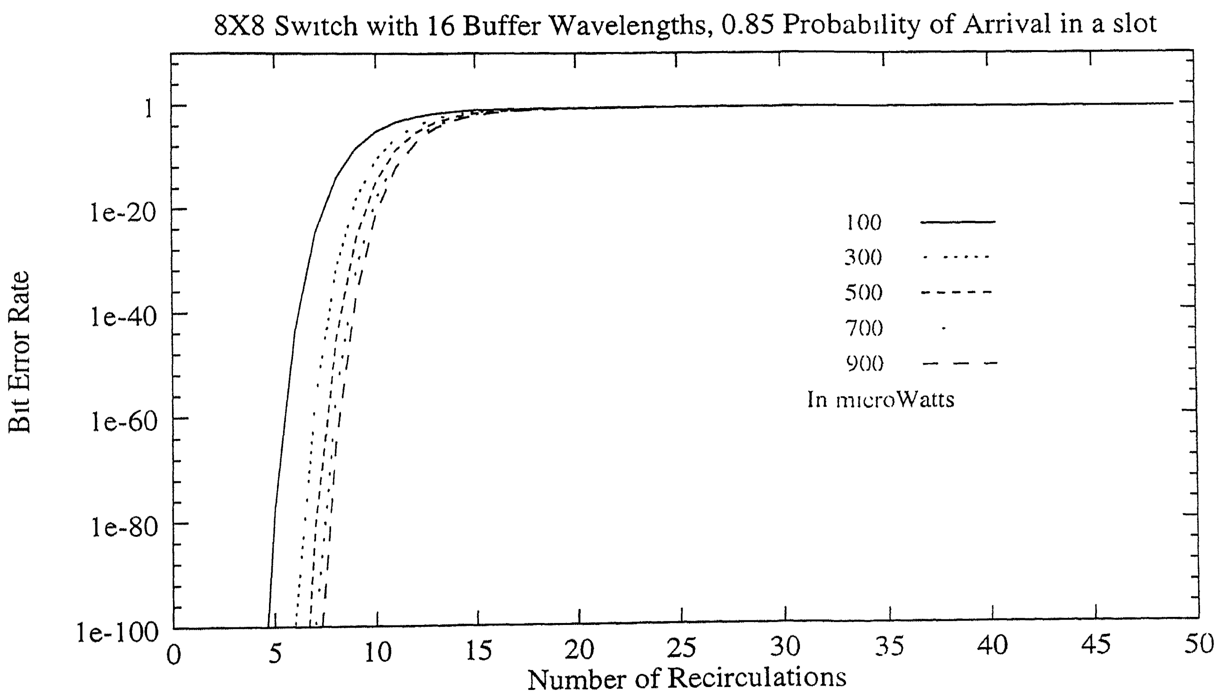

Figure 4.5. BER variation with number of recirculations With different input powers

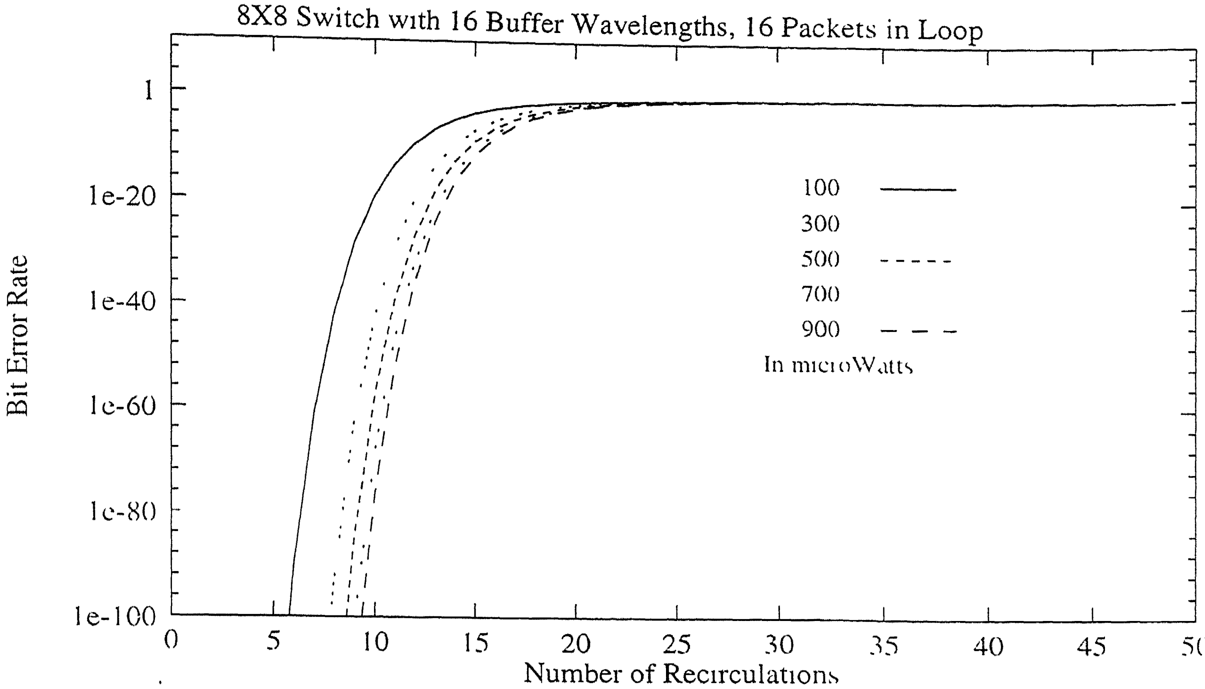

Figure 4.6 BER variation with number of recirculations for diff. input powers

which accumulates with the recirculations and increases the Bit Error Rate rapidly This is the reason for significant increase in BER with recirculations for low powers or less number of packets in loop.

For higher powers at the input of EDFA, the gain saturates to small value and so the ASE noise is also low. This low value of ASE allows the packet to stay in the loop for more number of recirculations. When the number of packets in loop are less, higher ASE noise is produced at early rotations, thus restricting the recirculation limit. For higher number of packets the EDFA input power level is high, thus giving better performance. This effect is more pronounced for more number of packets in loop.

For all the cases above it is seen that for single packet rotating in the loop, the performance is not good as the BER degrades very rapidly. The recirculation limit increases slightly with increase in input power. For higher loads or higher number of packets in loop the performance improves and the recirculation limit increases signifi-

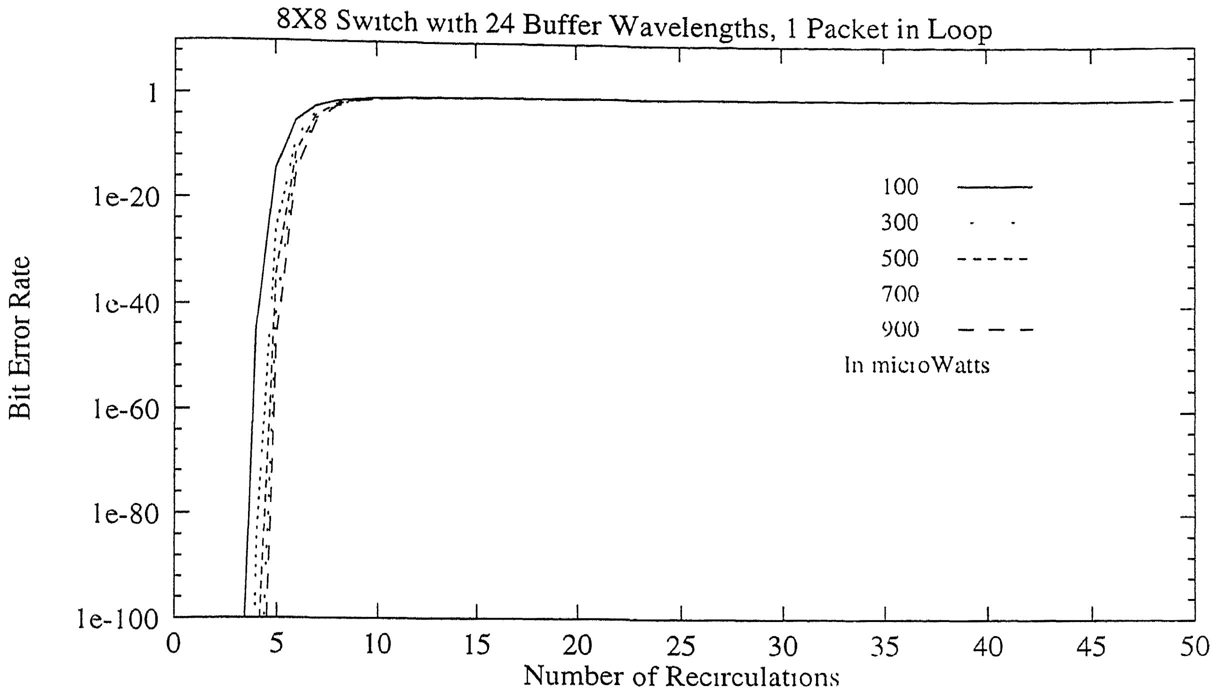

Figure 4.7: BER variation with number of recirculations for diff input powers

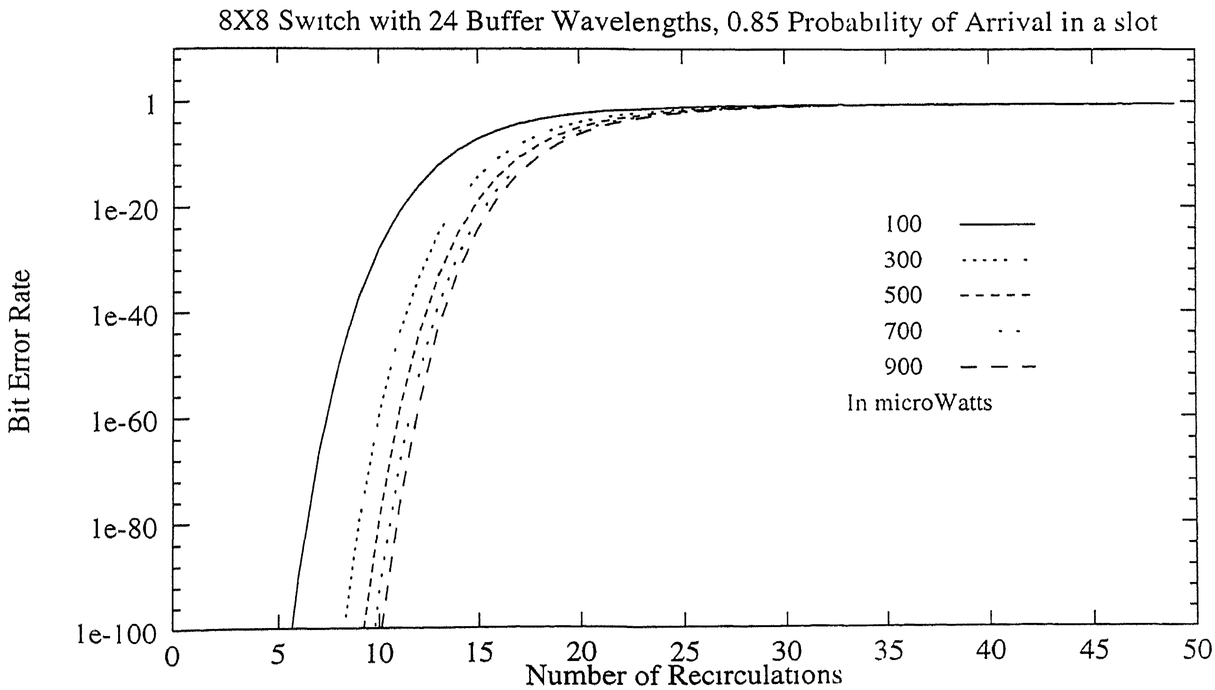

Figure 4.8: BER variation with number of recirculations for diff. input powers

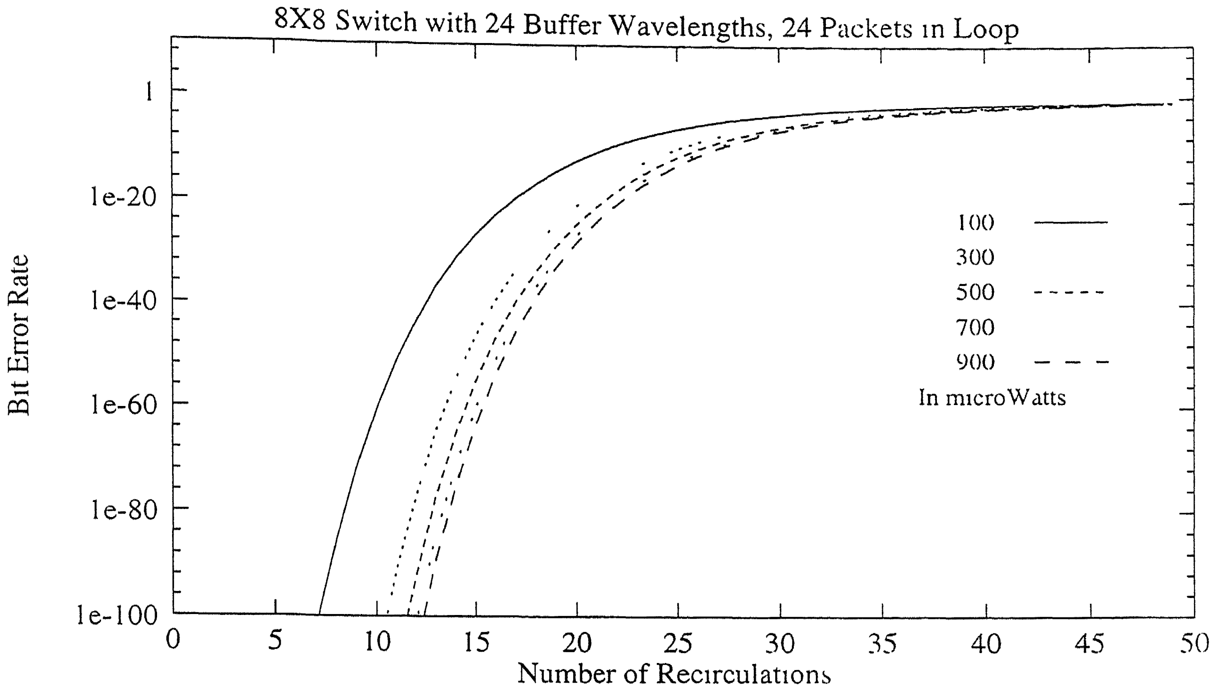

Figure 4.9: BER variation with number of recirculations for diff. input powers

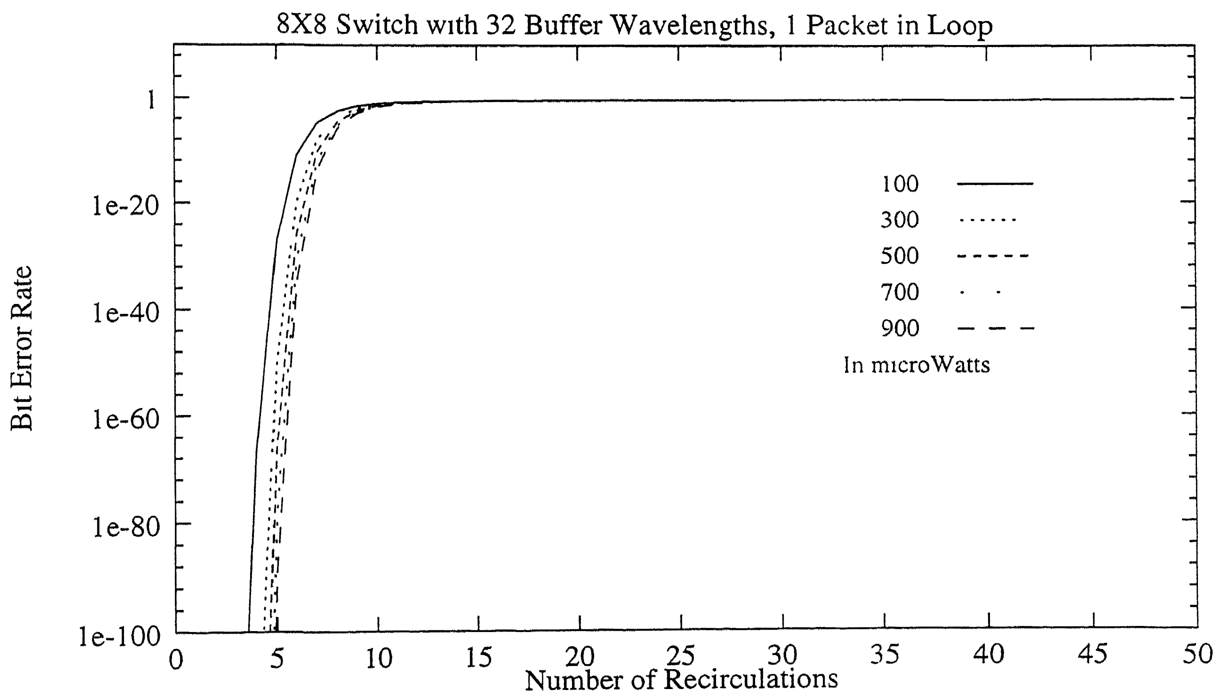

Figure 4.10: BER variation with number of recirculations for diff. input powers

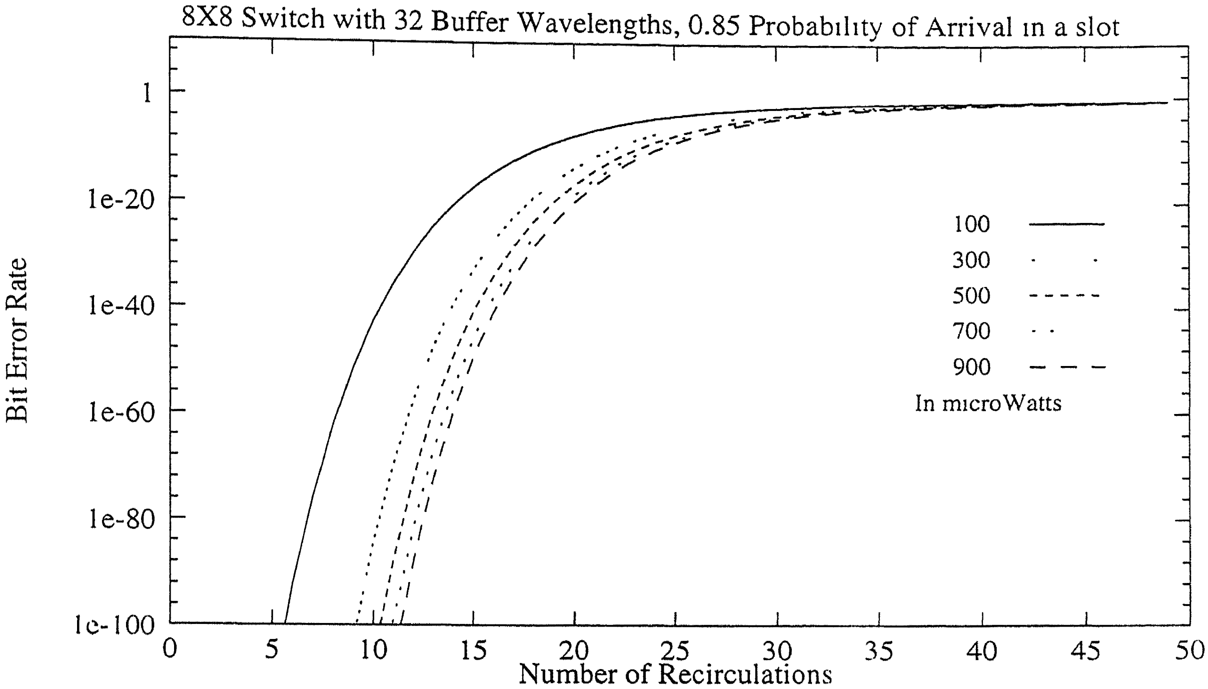

Figure 4.11: BER variation with number of recirculations for diff. input powers

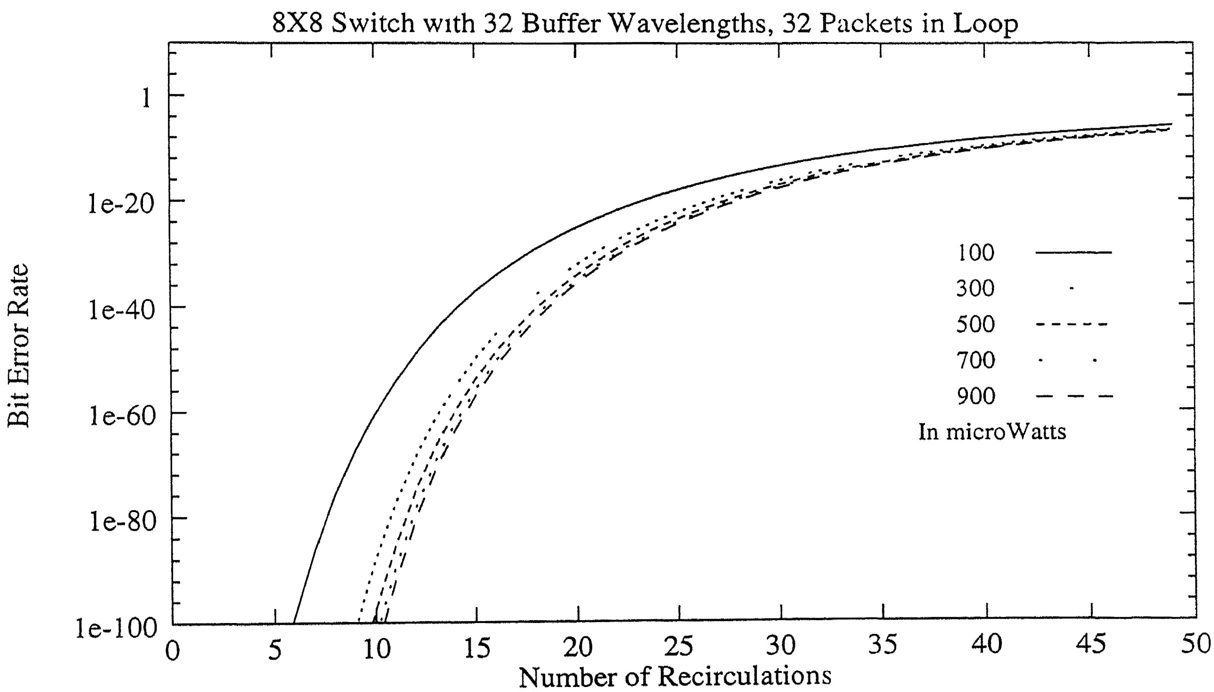

Figure 4.12: BER variation with number of recirculations for diff. input powers

cantly. Finally when the loop contains packets on all wavelengths, the performance is on its best.

8×8 switch was also observed without EDFA in the loop Without EDFA it was found that performance is very bad for more than 6 wavelengths in loop The reason is that total attenuation in the loop exceeds the unsaturated gain of SOA and thus signal gets attenuated very rapidly with the number of rotations

4.5 Observations for 16×16 switch

For 16×16 switch two cases with 24 and 32 channels in loop are considered. Fig 4 13, 4.14 and 4 15 are for 24 channels while Fig. 4.16, 4.17 and 4 18 are for 32 channels The observations are similar in all respects as those for 8×8 switch. It is seen that with increased number of packets in loop, the recirculation limit increases. The reason again, as explained in the previous section, is higher ASE noise accumulation for low input power or less number of packets in loop.

There is a small discrepancy in plots shown for 32 wavelengths. There is a slight decrease in Bit Error Rate after second recirculation. As it has already been explained that for low powers at EDFA's input, the gain is very large and also is the Noise, the power levels at the output of switch becomes very large. For the first rotation signal is attenuated significantly since it passes through a 16:1 combiner followed by DEMUX/MUX with 32 wavelengths each in the loop, followed by a 1:16 splitter, all of these account for heavy attenuation. Thus the power level at the input of EDFA in first rotation is very less, giving rise to very high gain, and hence at output of switch signal power is very high.

The Bit Error Rate does not depend directly on Signal to Noise Ratio, but it depends on the difference of signal powers for bit "1" and bit "0" and noise variances

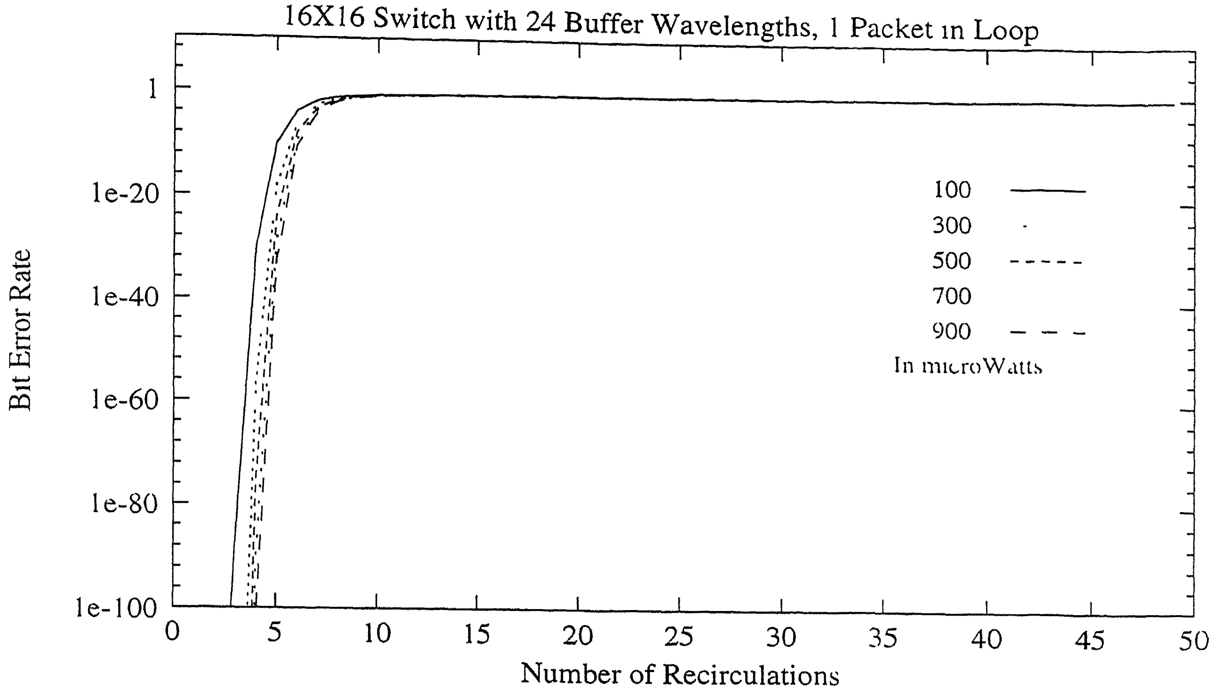

Figure 4.13: BER variation with number of recirculations for diff. input powers

Thus the unusual power levels at the output results in a slight discrepancy in the Bit Error Rate plot. This discrepency is not visible for higher powers At lower power levels, the amplification gives rise to increase in signal as well as noise. As the thermal noise becomes negligible, compared to ASE noise after amplification we see improvement. After certain number of recirculations, the system becomes ASE noise limited and degradation is observed.

4.6 Comparison of various switches

The comparison table for recirculation limit for all switches considered is shown in Fig. 4.19. It is seen that for an 8×8 switch with 32 wavelengths recirculation limit may be up to 38, when there is a packet on every wavelength. Similar recirculation limit is obtained for 16×16 switch with 32 wavelengths for packets on all wavelengths.

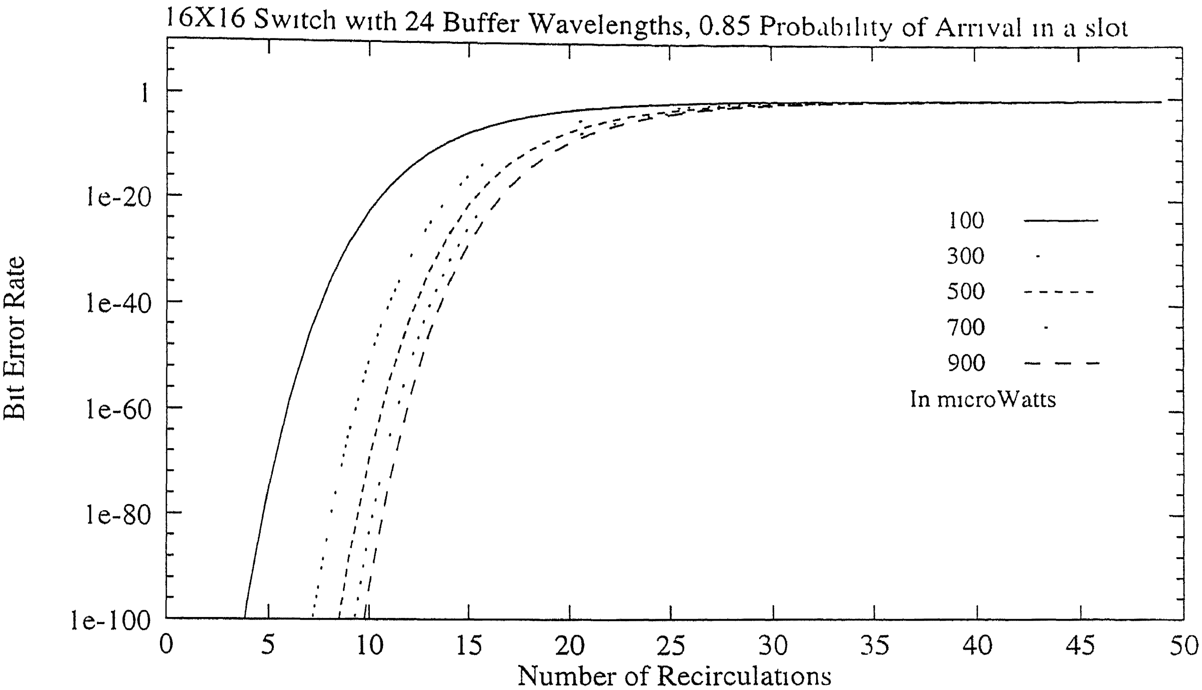

Figure 4 14: BER variation with number of recirculations for diff input powers

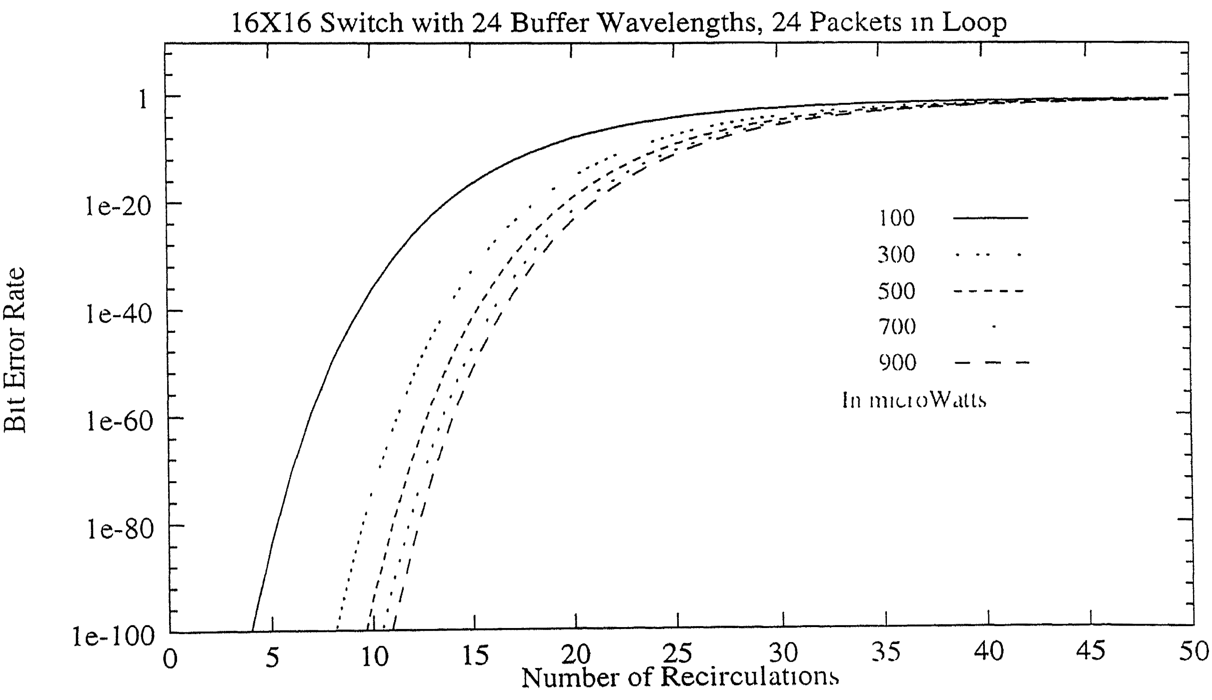

Figure 4.15: BER variation with number of recirculations for diff. input powers

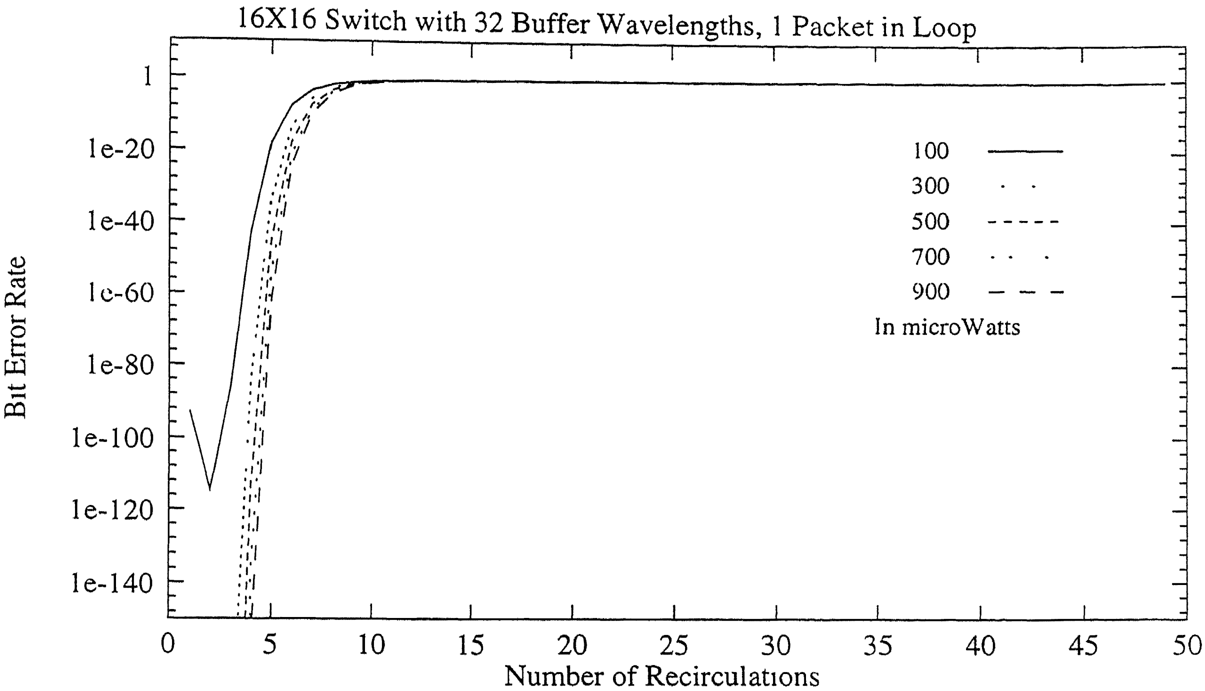

Figure 4.16: BER variation with number of recirculations for diff. input powers

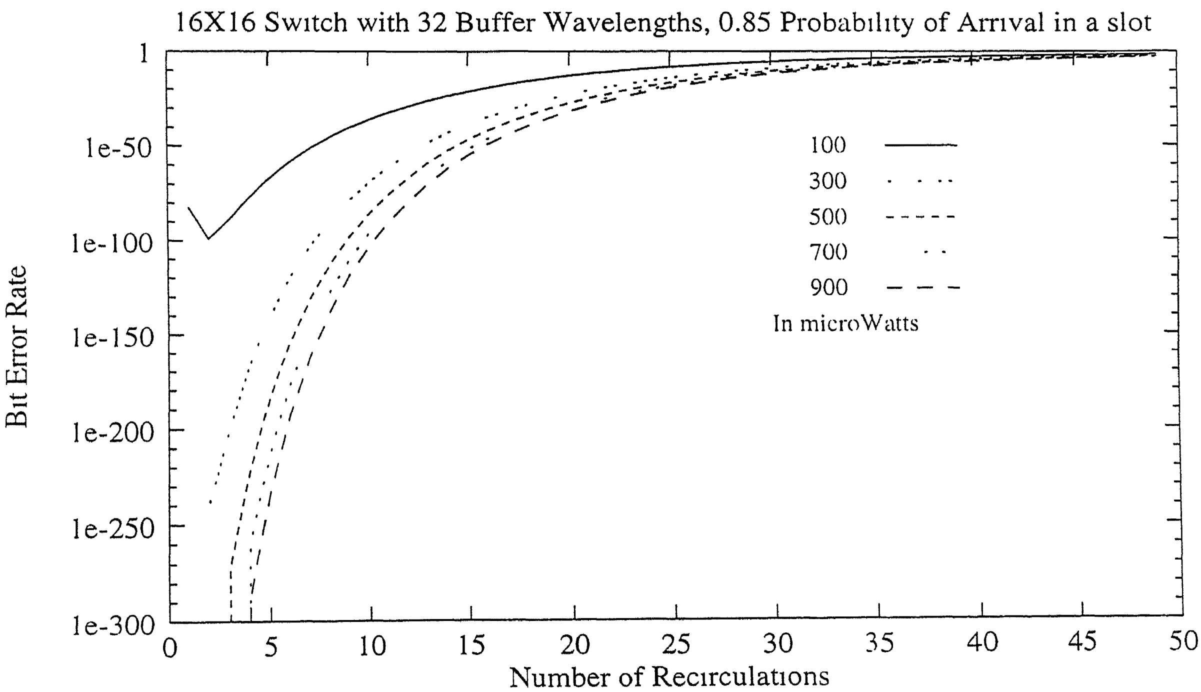

Figure 4.17: BER variation with number of recirculations for diff input powers

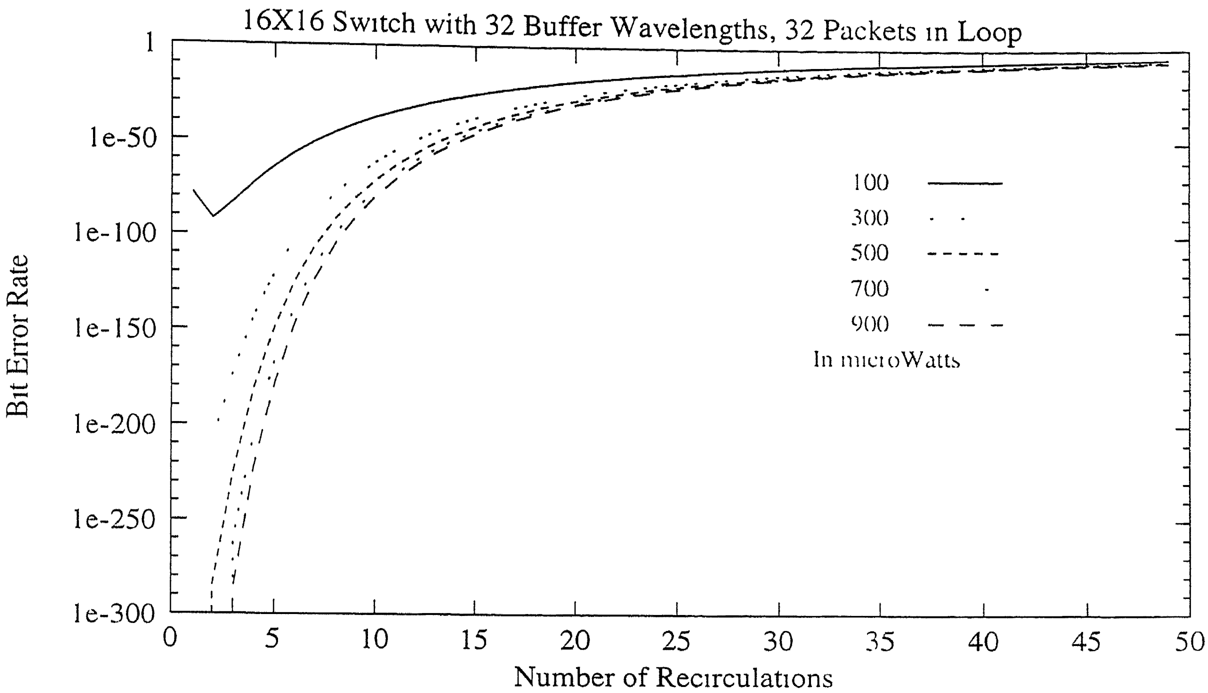

Figure 4.18: BER variation with number of recirculations for diff. input powers

S.N.	Switch Details			Recirculation Limit in Loop For various input powers, in micro Watts				
	Size	Buffer Wavelengths	Packets in Loop	100	300	500	700	900
1	8X8	16	1	4	4	5	5	5
2	8X8		9	8	9	10	10	11
3	8X8		16	11	13	14	14	15
4	8X8	24	1	5	5	6	6	6
5	8X8		14	13	15	16	17	17
6	8X8		24	20	24	25	25	26
7.	8X8	32	1	6	6	6	7	7
8.	8X8		16	17	21	22	23	23
9.	8X8		32	33	37	37	38	38
10.	16X16	24	1	4	5	5	5	5
11	16X16		17	13	16	17	18	19
12.	16X16		24	17	22	23	24	25
13.	16X16	32	1	5	6	6	6	6
14	16X16		24	21	27	29	30	30
15	16X16		32	28	34	35	36	36

Figure 4 19: Comparison Table for Recirculation Limit for various switches

Chapter 5

Conclusion and Future Scope

This work presented noise analysis of an All-Optical Packet Switch, based on multi-wavelength fiber loop memory switch architecture.

The first of our observations is that for increased switch size, the number of wavelengths required becomes large, thus large size switches are not possible due to unavailibility of large number of wavelength, although with the advancement in technology they are expected to increase.

Secondly we showed that the Bit Error Rate at the output of switch largely depends on the gain of EDFA. EDFA gain depends on the total power present at it's input which ultimately depends on the number of channels active in loop. The gain of EDFA is large for initial few rotations but it finally settles to some lower value after some recirculations, so that the total gain in the loop is equal to the total loss.

If the power to EDFA's input is very small then its gain is very high, and therefore the ASE noise due to EDFA is also high. This noise accumulates with recirculations and degrades the BER performance very rapidly. Hence the recirculation limit is less. If the input power to EDFA is such that the gain is close to this final value, then the

ASE noise produced is not very high, hence the recirculation limit becomes large.

Hence we conclude that for large number of packets in loop, the recirculation limit gets better . This limit is around 35 rotations for both 8×8 switch as well as for 16×16 switch with 32 wavelengths when there is a packet on each wavelength We can make a general remark that for an efficient all optical packet switch, the gain of EDFA and SOA should be maintained just equal to total loss in the loop This will give maximum number of recirculations possible.

Future Scope

- In this work Bit Error Rate performance of a single switch is considered. This can be extended to multiple switches interconnected with one another Exhaustive simulations are required to obtain the performance of a switch in such network.
- The performance is further expected to improve if a preamplifier in introduced at the receiver. Similar analysis can be carried out with preamplifier.
- One can investigate the strategies to maintain amplifier gain just equal to total loss in the loop, so that the optimal performance of loop can be achieved.

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